Service Guide

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For Safety information, Warranties, and Regulatory information, see the pages at the end of the book.

Agilent Technologies 16517A/18A 4 GSa/s Timing and 1 GSa/s Synchronous State Logic Analyzer

Agilent Technologies 16517A/18A

The Agilent Technologies 16517A/18A is a 4 GSa/s timing, 1 GSa/s synchronous state logic analyzer module for the Agilent Technologies 16500A/B Logic Analysis system. The 16517A is the Master Card; it offers the minimum configuration of 16 channels (8 channels in half-channel mode) with 1 clock input. The 16518A is an Expansion Card, which requires the 16517A Master Card. Up to four 16518As can be connected, to provide a total of 80 channels of data aquisition (40 channels in half-channel mode).

Features

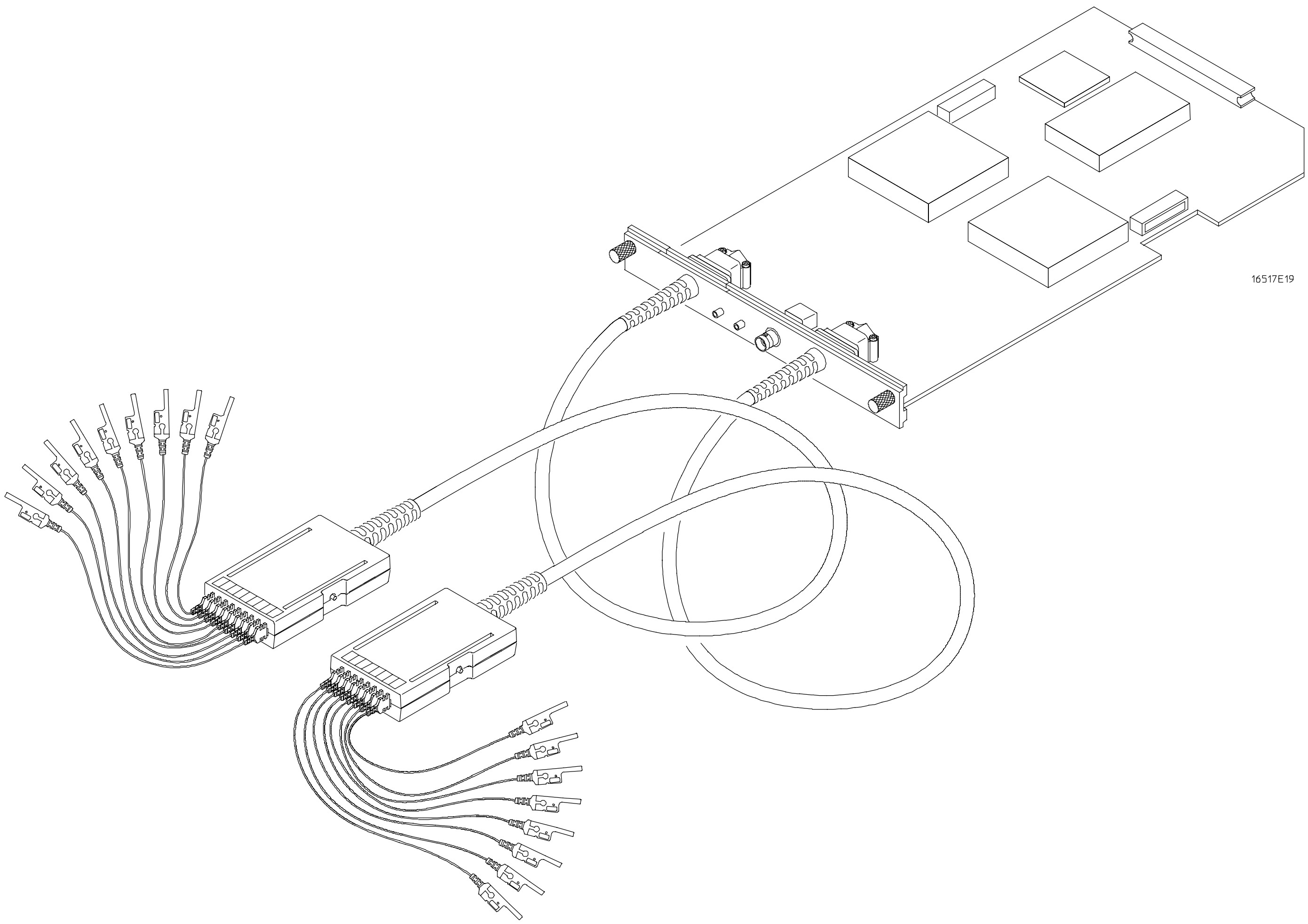
Some of the main features of the 16517A/16518A are as follows:

- 4 GSa/s timing analysis, providing up to 250 ps resolution
- 1 GHz synchronous state analysis, providing up to 2 GSa/s synchronous state analysis
- 16 channels per 16517A Master Card, 16 channels per 16518A Expansion Card, and a maximum of 80 channels per Agilent Technologies 16500 Logic Analysis System
- 64 Kbits memory per channel (128 Kbits per channel in half-channel mode)
- Pattern, pattern duration, branching, edge, arm trigger between modules via Intermodule Bus
- Small, lightweight probing, with 500 Ohm impedance at 1 GHz

Service Strategy

The service strategy for this instrument is the replacement of defective assemblies. This service guide contains information for finding a defective assembly by testing and servicing the 16517A/18A.

This instrument can be returned to Agilent Technologies for all service work, including troubleshooting. Contact your nearest Agilent Technologies Sales Office for more details.



The 16517A Master Card

In This Book

This book is the service guide for the Agilent Technologies 16517A/18A 4 GSa/s Timing, 1 GSa/s Synchronous State Logic Analyzer. Place this service guide in the 3-ring binder supplied with your *Agilent Technologies 16500 Logic Analysis System Service Guide*.

This service guide is divided into eight chapters.

Chapter 1 contains information about the instrument and includes accessories for the instrument, specifications and characteristics of the instrument, along with a list of the equipment required for servicing the instrument.

Chapter 2 tells how to prepare the instrument for use.

Chapter 3 gives instructions on how to test the performance of the instrument.

Chapter 4 contains calibration and adjustment instructions for the instrument.

Chapter 5 contains self-tests and flowcharts for troubleshooting the instrument.

Chapter 6 tells how to replace the instrument and assemblies of the instrument and how to return them to Agilent Technologies.

Chapter 7 lists replaceable parts, shows an exploded view, and gives ordering information.

Chapter 8 explains how the instrument works and what the self-tests are checking.

Contents

4 Calibrating and Adjusting

5 Troubleshooting

6 Replacing Assemblies

1

General Information

General Information

This chapter lists the accessories, the specifications and characteristics, and the recommended test equipment.

Accessories

The following accessories are supplied with the 16517A/18A Logic Analyzer.

Accessories Supplied	Agilent Part Number	Qty
Composite operating software	16517-69501	
Accessory Master Kit	16517-68701	(includes items listed below)
SMT Kit	16517-82104	4 black, 4 red
GND Extender Kit	16517-82105	20
GND Lead Kit	16517-82106	20
Pin-Probe Kit	16517-82107	4
Grabber Kit	16517-82108	20
Adapter Cable, BNC-SMB	16517-61604	1
Calibration Pod	16517-63201	1
Accessory Expander Kit	16518-68701	(includes items listed above except for Adapter Cable BNC-SMB and Calibration Pod)

An illustration of the parts in the accessory kits is shown in chapter 7.

Accessories Available	Agilent Part Number	Qty
Adapter, HST-to-SMA (high speed timing)	16517-27601	1
Adapter, HST-to-BNC	16517-27602	1
Probe Replacement Kit	5081-7753	1

Other accessories available for the 16517A/18A Logic Analyses are listed in the *Accessories for Agilent Logic Analyzers* brochure.

Specifications

The specifications are the performance standards against which the product is tested. They are specified for an input signal VH = –0.9V, VL = –1.7V, slew rate = 1V/ns, and threshold = –1.3V.

Minimum Input Voltage Swing: 500 mV peak to peak.

Threshold Accuracy: ± 2% of input signal ± 50 mV.

Minimum External Clock Period: 1 ns.

Setup/Hold:

Per pod*	350 ps/350 ps.
Across pods	750 ps/750 ps.
	350 ps/350 ps, with manual deskew.

Actual setup/hold adjustable with sample offset in all modes.

* For the frequency range of 62.5 MHz to 20 MHz, a duty cycle of 40% to 60% is required.

Characteristics

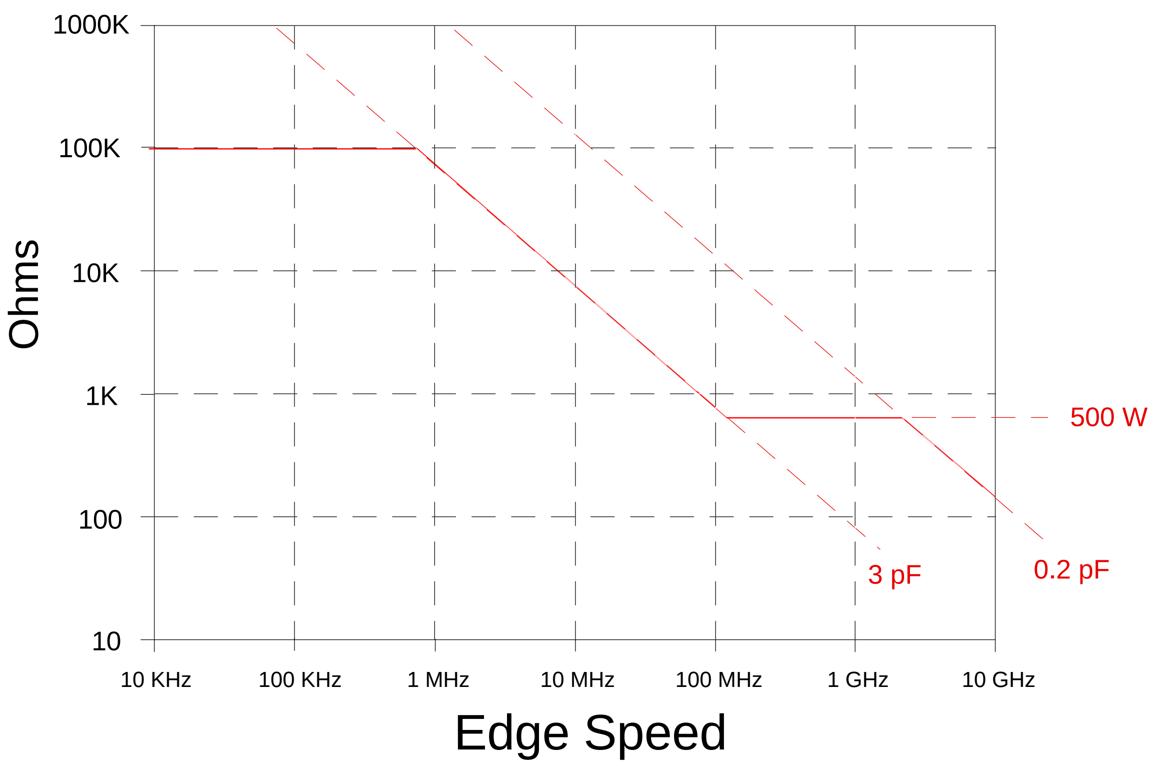
These characteristics are not specifications, but are included as additional information. The following characteristics are typical for the 16517A/18A.

Probes

Input DC Resistance: 100 KΩ, ± 2%.

Input Impedance:

DC thru 400 ns rise time	100 KΩ, typical.
3.5 ns thru 350 ps	500 Ω, typical.



Impedance Curve

Input Capacitance: 0.2 pF and then, through 500 Ω, 3 pF.

Minimum Input Overdrive: 250 mV or 30% of input (whichever is greater) above the pod threshold.

Threshold Range Increments: ±5.0 V in 10 mV increments.

Threshold Setting: Preset TTL, ECL, or User-defined on a per pod basis.

Input Dynamic Range: ±5 V about the threshold.

Maximum Input Voltage: 40 V peak-to-peak.

Synchronous State Analysis

Maximum External Clock Speed: 1 GHz, requires a periodic clock.

Minimum State Speed: 20 MGSa/s, requires a periodic clock.

Minimum Detectable Pulse Width: 900 ps.

Channel Count: 16 per card, up to 80 in one frame.

Channel-to-Channel Skew across up to 80 channels:

Per pod	250 ps, typical.
Across pods	1 ns, typical.
	250 ps, with manual deskew.

Memory Depth per Channel: 65536 samples.

State Clocks: One external clock is available on the master board. No clocks are available on the expander board. Clock edge is selectable as positive or negative.

State Clock Duty Cycle Range:

1 GHz thru 500 MHz	45% - 55%, typical.
500 MHz thru 250 MHz	30% - 70%, typical.
250 MHz thru 20 MHz	20% - 80%, typical.

Oversampling: 2x, 4x, 8x, 16x, and 32x, with a maximum rate of 2 GSa/s.

Timing Analysis

Timing Modes: Conventional timing.

Timing Speed: 15.3 KSa/s – 2 GSa/s full channel, 4 GSa/s half channel.

Sample Period: 500/250 ps minimum (full/half channel mode), 65.536 us maximum.

Channel Count: 16/8 per card (full/half channel mode).

Minimum Detectable Pulse Width:

4 GSa/s	800 ps, typical.
2 GSa/s or less	1.1 ns, typical.

Memory Depth per Channel: 65536 samples full channel mode, 131072 samples, half channel mode.

Time Covered by Data: 32.8 us at 2 GSa/s or 4 GSa/s up to 4.3 s at 15.3 KSa/s.

Time Interval Accuracy: ± (sample period + channel-to-channel skew + 0.005% of time interval reading).

Sample Period Accuracy: 0.005% of sample period.

Channel-to-Channel Skew across up to 80 channels: 250 ps, typical.

Maximum Delay After Triggering: (2 to the 20th)*(sample period) or 16.78 ms at or below 16 ns sample period.

Note: When oversampling, use oversampled period for sample period above.

Trigger Characteristics

Pattern Recognizers: 4. Each pattern recognizer is the AND combination of bit (0, 1, or X) patterns.

Pattern Width: 16/32/48/64/80 channels.

Minimum Pattern Recognizer Pulse Width: 2.25 ns.

Edge Recognizers (Timing only): 2. Trigger on a rising, falling, or either edge on any channel. Edges are OR'd across all channels.

Edge Width: 16/32/48/64/80 channels.

Edge Counting Frequency: 444 MHz.

Edge Detection: Up to 1 GHz.

Greater than Duration (Timing only): 0 nsec to 510 nsec range, accuracy is ± 2.25 ns.

Less than Duration (Timing only): 4 nsec to 510 nsec range, accuracy is ± 2.25 nsec.

Qualifier: A user-specified term that can be any state, no state, any recognizer (patterns or edges), the timer, or the logical combination (AND, OR, XOR) of the recognizers and timers.

Branching: Each sequence level has two branching qualifiers. When satisfied, the analyzer will branch to the specified sequence level.

Maximum Occurrence Count: 16,777,216.

Maximum Sequencer Speed: 500 MHz.

State Sequence Levels: 4 plus trace point.

Timing Sequence Levels: 4 plus trace point.

Timer/Counter: There is one timer or counter per sequence level, which is restarted upon each entry into each level.

Timer/Counter Range:

Timing mode	0 s to 33 ms.
State mode	500 MHz to 1 GHz, (user clock period)*(2 to the 23rd).
	below 500 MHz, (user clock period)*(2 to the 24th).

Timer Resolution:

Timing mode	2 ns.
State mode	above 500 MHz, 2 X user clock period.
	below 500 MHz, user clock period.

Timer Accuracy: 0.005% of timer value.

Measurement and Display Functions

Arming: Can be armed by the Run key, the external SMB, or the Intermodule Bus (IMB).

Trace Mode: Single mode acquires data once per trace specification. Repetitive mode repeats single mode acquisitions until Stop is pressed or until pattern time interval or compare stop criteria are met.

Labels: Channels may be grouped together and given a 6-character name. Up to 126 labels in each analyzer may be assigned with up to 32 channels per label. Trigger terms may be given an 8-character name.

Activity Indicators: Provided in the Format menu for monitoring device-under-test activity while setting up the analyzer. The indicators only function when the analyzer is stopped.

Pod ID: A button provided on each pod which, when pressed, causes the display of its slot letter and pod number on the analyzer screen.

Markers: Two markers (X and O) are shown as dashed lines in the display.

Trigger: Displayed as a red vertical dashed line in the waveform display and as line 0 in the listing and compare displays.

Measurement Functions

Run: Starts acquisition of data in specified trace mode.

Stop: In single trace mode or the first run of a repetitive acquisition, Stop halts acquisition and displays the current acquisition data. For subsequent runs in repetitive mode, Stop halts acquisition of data and does not change current display.

Time Interval: The X and O markers measure the time interval between events.

Patterns: The X or O marker can be used to locate the nth occurrence of a specified pattern before or after trigger, or after the beginning of data. The O marker can also find the nth occurrence of a pattern before or after the X marker.

Statistics: X to O marker statistics are calculated for repetitive acquisitions. Patterns must be specified for both markers, and statistics are kept only when both patterns can be found in an acquisition. Statistics are minimum X to O time, maximum X to O time, average X to O time, and ratio of valid runs to total runs.

Compare Mode Functions: Performs a post-processing bit-by-bit comparison of the acquired state data and Compare Reference data.

Compare Reference: Created by copying an acquisition into the compare reference buffer. Allows editing of any bit in the Compare Reference to a 1, 0 or X.

Compare Reference Boundaries: Each channel (column) in the compare reference can be enabled or disabled via bit masks. Upper and lower ranges of states (rows) in the compare reference can be specified. Any data bits that do not fall within the enabled channels and the specified range are not compared.

Stop Measurement: Repetitive acquisitions may be halted when the comparison between the current acquisition and the Compare Image is equal or not equal.

Compare Mode Display: Reference Listing display shows the Compare Reference and bit masks. Difference Listing display highlights differences between the current acquisition and the Compare Reference.

Data Entry/Display

Display Modes: Listing, Waveform, Compare Reference Listing, and Compare Difference Listing. Time-correlated oscilloscope traces can also be displayed in the waveform display mode when the intermodule bus is used.

Markers: Correlated to listing, and waveform displays. Available as pattern, time, or statistics.

Waveform Displays: Display acquisition in waveform format.

Sec/div: 250 ps to 50 s.

Delay: –2,500 s to +2,500 s.

Accumulate: Waveform display is not erased between successive acquisitions.

Overlay Mode: Multiple channels can be displayed on one waveform display line. When waveform size is set to large, the value represented by the waveforms is displayed inside the waveforms in selected base.

Displayed Waveforms: 24 lines maximum on one screen. Up to 96 lines may be specified and scrolled through.

Bases: Binary, Octal, Decimal, Hexadecimal, ASCII (data displays only), User-defined symbols, and two's compliment.

Pattern Symbols: User can define a mnemonic for the specific bit pattern of a label. When label base is SYMBOL, mnemonic is displayed where the bit pattern occurs.

Range Symbols: User can define a mnemonic covering a range of values. When data display is SYMBOL, values within the specified range are displayed as mnemonic + offset from base of range.

Number of Symbols: 1000 maximum.

Recommended Test Equipment

Equipment Required

Equipment	Critical Specifications	Recommended Agilent Model/Part	Use*
Pulse Generator	1 GHz, 600 ps rise time	8131A Option 020	P
Digitizing Oscilloscope	> 6 GHz bandwidth, <58 ps rise time	54121T	P
Oscilloscope Probe	20:1, ≥6 GHz bandwidth	54006A	
Digitizing Oscilloscope	≥ 500 MHz bandwidth	54520A	P, T
Oscilloscope Probe	10:1, ≥500 MHz bandwidth	10441A	
DC Power Supply	DC Offset Voltage ±5.2V dc, 1 mV resolution	3325B Option 002 **	P
Digital Multimeter	0.1 mV resolution, 0.005% accuracy	3458A	P
Calibration Module	No Substitute	16517-63201	A, P
BNC-Banana Cable	≥ 1 GHz bandwidth	11001-60001	P
BNC Tee	BNC (m)(f)(f)	1250-0781	P
BNC Coax Cable		10503A	A, P
SMA Coax Cable	18 GHz bandwidth	8120-4948	P, T
Adapter	SMA(m)-BNC(f)	1250-1200	P
Adapter	SMA(f)-BNC(m)	1250-2015	P

* A = Adjustment P = Performance Tests T = Troubleshooting

** Any DC power supply which meets the critical specifications can be used; however, the procedures are written for the 3325B option 002

Preparing for Use

Preparing For Use

This chapter gives you instructions for preparing the logic analyzer module for use.

Power Requirements

All power supplies required for operating the logic analyzer are supplied through the backplane connector in the mainframe.

Operating Environment

The operating environment is listed in chapter 1. Note the noncondensing humidity limitation. Condensation within the instrument can cause poor operation or malfunction. Provide protection against internal condensation.

The logic analyzer module will operate at all specifications within the temperature and humidity range given in chapter 1. However, reliability is enhanced when operating the module within the following ranges:

- Temperature: +20 °C to +35 °C (+68 °F to +95 °F)
- Humidity: 20% to 80% noncondensing

Storage

Store or ship the logic analyzer in environments within the following limits:

- Temperature: –40 °C to + 75 °C
- Humidity: Up to 90% at 65 °C
- Altitude: Up to 15,300 meters (50,000 feet)

Protect the module from temperature extremes which cause condensation on the instrument.

To inspect the module

1 **Inspect the shipping container for damage.**

If the shipping container or cushioning material is damaged, keep them until you have checked the contents of the shipment and checked the instrument mechanically and electrically.

2 **Check the supplied accessories.**

Accessories supplied with the module are listed in "Accessories" in chapter 1.

3 **Inspect the product for physical damage.**

Check the module and the supplied accessories for obvious physical or mechanical defects. If you find any defects, contact your nearest Agilent Technologies Sales Office. Arrangements for repair or replacement are made, at Agilent Technologies' option, without waiting for a claim settlement.

To prepare the mainframe

CAUTION Turn off the mainframe power before removing, replacing, or installing the module.

CAUTION Electrostatic discharge can damage electronic components. Use grounded wriststraps and mats when performing any service to this module.

1 Turn off the mainframe power switch, then unplug the power cord. Disconnect any input or output connections.

2 Plan your module configuration.

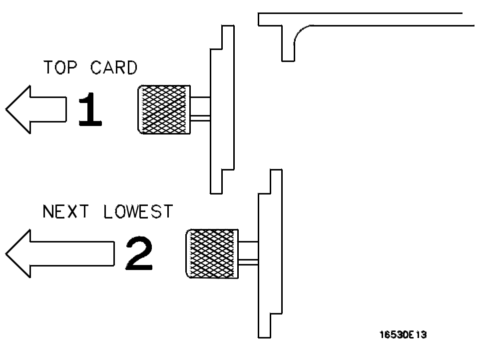
If you are installing a one-card module, use any available slot in the mainframe.

If you are installing a multicard module, use adjacent slots in the mainframe. See illustration on next page for multicard combinations.

3 Loosen the thumb screws.

Cards or filler panels below the slots intended for installation do not have to be removed.

Starting from the top, loosen the thumb screws on filler panels and cards that need to be moved.



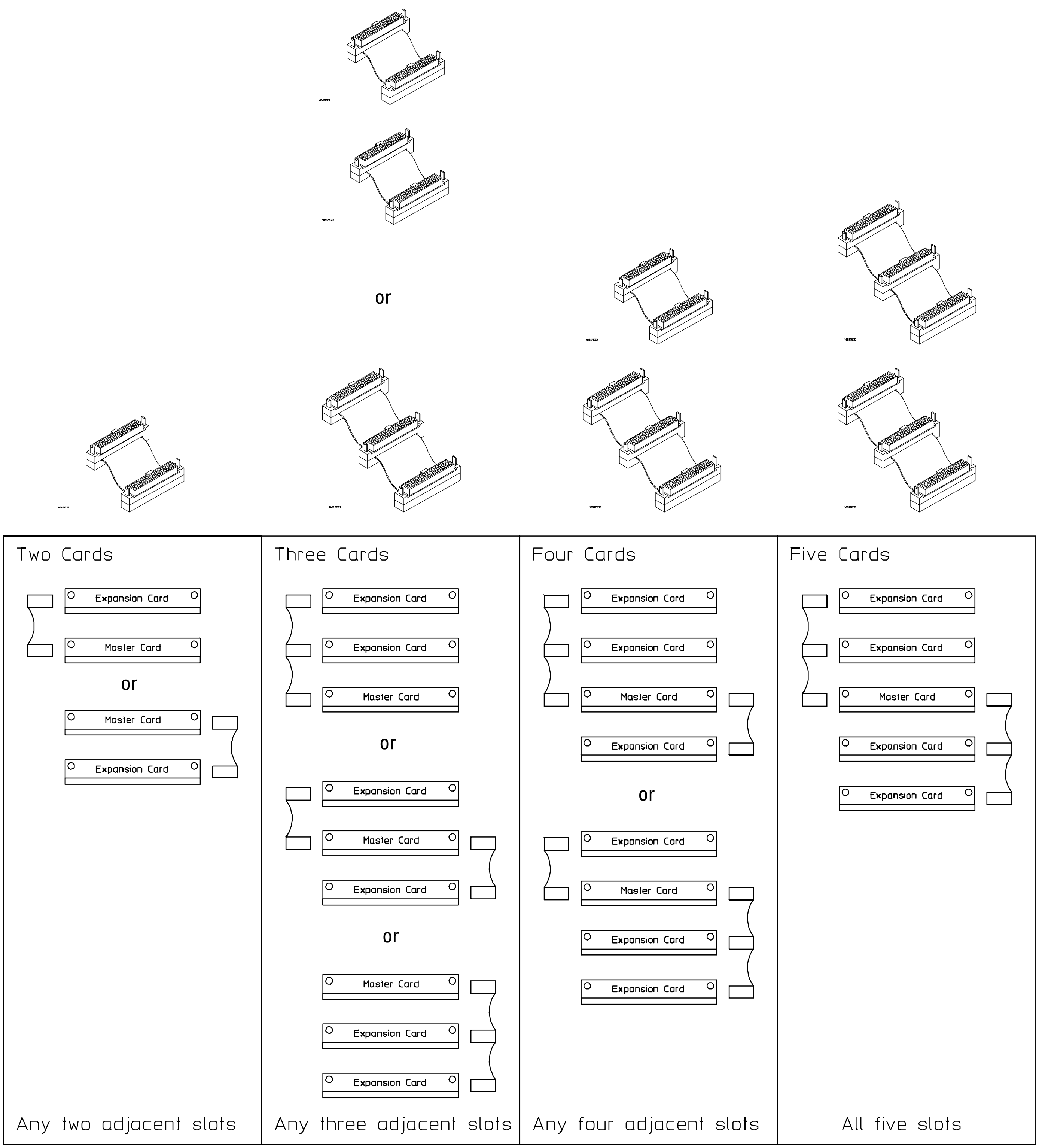
4 Starting from the top, pull the cards and filler panels that need to be moved halfway out.

CAUTION All multicard modules will be cabled together. Pull these cards out together to prevent damage to the cables and connectors. See Chapter 6 for information on removing cables.

5 Remove the cards and filler panels.

Remove the cards or filler panels that are in the slots intended for the module installation. Push all other cards into the card cage, but not completely in. This is to get them out of the way for installing the module.

Some modules for the Logic Analysis System require calibration if you move them to a different slot. For calibration information, refer to the manuals for the individual modules.


or
Two Cards
Expansion Card
Master Card
or
Master Card
Expansion Card
Any two adjacent slots
Three Cards
Expansion Card
Expansion Card
Master Card
or
Expansion Card
Master Card
Expansion Card
or
Master Card
Expansion Card
Expansion Card
Any three adjacent slots
Four Cards
Expansion Card
Expansion Card
Master Card
Expansion Card
or
Expansion Card
Master Card
Expansion Card
Expansion Card
Any four adjacent slots
Five Cards
Expansion Card
Expansion Card
Master Card
Expansion Card
Expansion Card
All five slots

16517M01

To configure a one-card module

- The 16517A module can be used as a one-card module. The 16518A module cannot be used as a one-card module.
- If you need to configure a multicard module into a one-card module, remove the cables connecting the cards (see chapter 6 for removing cables).

To configure a multicard module

To configure a multicard module, connect the cables as follows:

> Save unused cables for future configurations.

- To configure a two-card module, use the short cable to connect the 16517A Master Card to the 16518A Expansion Card. Any of the two-card configurations shown in the illustration on page 2-4 can be used. The master card can be above or below the expansion card. Note that if the master card is below, the connector on the left side of the master card (when looking at back of mainframe) must be used; when the master card is above the expansion card, the connector on the right side of the master card must be used. See "To install the module" for the installation procedure.
- To configure a three-card module, you can have the master card in between the expansion cards, or above or below the expansion cards (see illustration on page 2-4). Note the cables which are used for each configuration, and the side of the master card which is used for connecting. If the master card is below, the connector on the left side of the master card (when looking at back of mainframe) must be used; when the master card is above the expansion card, the connector on the right side of the master card must be used. See "To install the module" for the installation procedure.
- To configure a four-card module, you can have one expansion card above the master card and two below, or two expansion cards above and one below (see illustration on page 2-4). Note the cables which are used for each configuration, and the side of the master card which is used for connecting. If the master card is below the expansion card, the connector on the left side of the master card (when looking at back of mainframe) must be used; when the master card is above the expansion card, the connector on the right side of the master card must be used. See "To install the module" for the installation procedure.
- To configure a five-card module, the master card must go in the middle slot, and two expansions cards are above it and two are below it (see illustration on page 2-4). The two long cables (three connectors) must be used. For the expansion cards above the master card, use the connector on the left side of the master card (when looking at back of mainframe); for the expansion cards below the master card, the connector on the right side of the master card must be used. See "To install the module" for the installation procedure.

To install the module

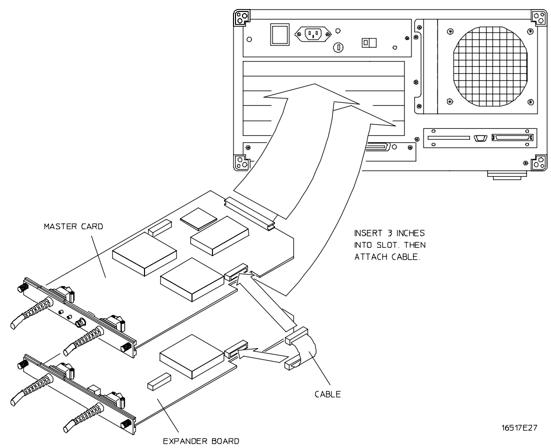
1 Slide the cards above the slots for the module about halfway out of the mainframe.

2 If the module consists of a single card, then slide the module approximately halfway into the mainframe.

If the module consists of more than one card, then perform the following steps:

a Slide the card approximately three inches into the mainframe.

b Connect the appropriate interface cable (long or short) to the appropriate side of the card (see illustration on page 2-4). Repeat steps a and b for the remaining cards.



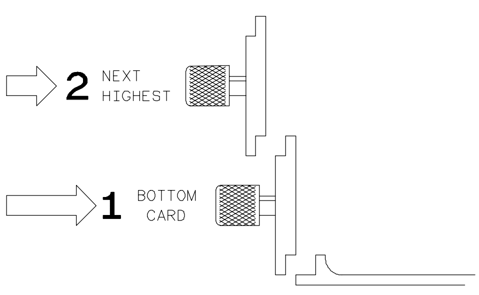
3 Slide the complete module into the mainframe, but not completely in.

Each card in the instrument is firmly seated and tightened one at a time in step 5.

4 Position all cards and filler panels so that the endplates overlap.

5 Seat the cards and tighten the thumbscrews.

Starting with the bottom card, firmly seat the cards into the backplane connector of the mainframe. Keep applying pressure to the center of the card endplate while tightening the thumbscrews finger-tight. Repeat this for all cards and filler panels starting at the bottom and moving to the top.



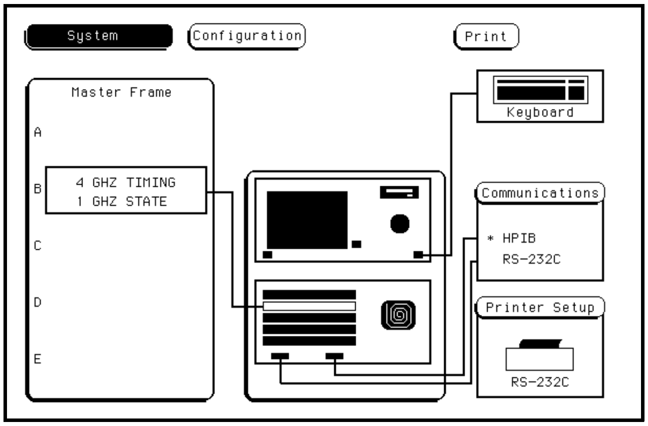
WARNING For correct air circulation, filler panels must be installed in all unused card slots. Correct air circulation keeps the instrument from overheating. Keep any extra filler panels for future use.

To turn on the system

1 Connect the power cable to the mainframe.

2 Turn on the power switch.

When you turn on the power switch, the logic analyzer performs power-up tests that check mainframe circuitry. After the power-up tests are complete, the screen will look similar to the sample screen below.



To test the module

- If you require a test to initially accept the operation, perform the self tests in chapter 3.
- If you need to deskew the channel-to-channel variations, go to chapter 4, "Calibrating and Adjusting."
- If you require a test to verify the specifications, start at the beginning of chapter 3, "Testing Performance."
- If the module does not operate correctly, go to the beginning of chapter 5, "Troubleshooting."

3

Testing Performance

Testing Performance

This chapter tells you how to test the performance of the logic analyzer against the specifications listed in chapter 1. To ensure the logic analyzer is operating as specified, software tests (self-tests) and manual performance tests are done on the module. The logic analyzer is considered performance-verified if all of the software tests and manual performance tests have passed. The procedures in this chapter indicate what constitutes a "Pass" status for each of the tests.

Test Strategy

For a complete test, start at the beginning with the software self tests and continue through to the end of the chapter. Ensure that the channel-to-channel variations have been deskewed before doing the performance verification tests (see chapter 4). For an individual test, follow the procedure in the test.

The performance verification procedures starting on page 3–10 are each shown from power-up. To exactly duplicate the set-ups in the tests, save the power-up configuration to a file on a disk, then load that file at the start of each test.

If a test fails, check the test equipment set-up, check the connections, and verify adequate grounding. If a test still fails, there is most likely a hardware problem.

Test Interval

Test the performance of the module at two-year intervals, or if it is replaced or repaired.

Performance Test Record

A performance test record for recording the results of each procedure is located at the end of this chapter. Use the performance test record to gauge the performance of the module over time.

Test Equipment

Each procedure lists the recommended test equipment. You can use equipment that satisfies the specifications given. However, the procedures are based on using the recommended model or part number.

Instrument Warm-Up

Before testing the performance of the module, warm-up the instrument and the test equipment for 30 minutes.

Initial Acceptance

If you require a test to initially accept the operation of the logic analyzer, perform the self-tests. Refer to "To perform the self-tests" in this chapter.

To make the test connectors

The test connectors connect the logic analyzer to the test equipment.

Materials Required

Description	Recommended Agilent Part	Qty
BNC (f) Connector	1250-1032	5
100 Ω 1% resistor	0698-7212	8
Berg Strip, 9-by-2		1
Berg Strip, 6-by-2		2
20:1 Probe	54006A	1
Jumper wire		

1 Build two test connectors using BNC connectors and 6-by-2 sections of Berg strip.

a Solder a jumper wire to all pins on one side of the Berg strip.

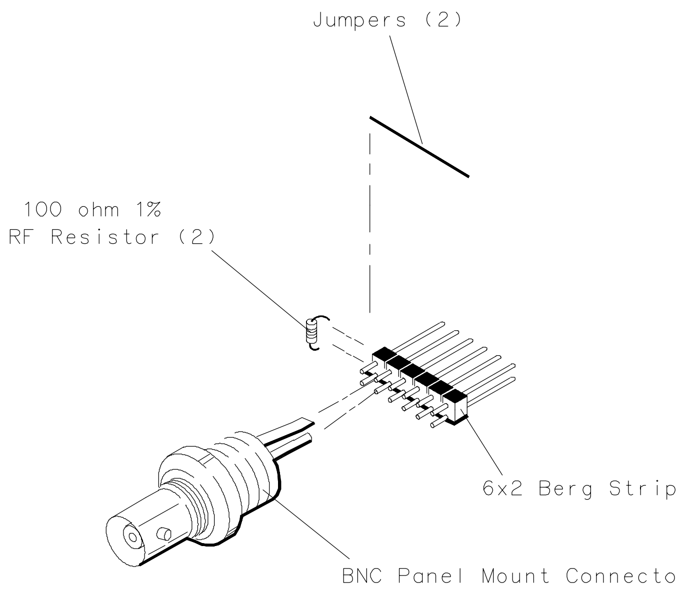
b Solder a jumper wire to all pins on the other side of the Berg strip.

c Solder two resistors to the Berg strip, one at each end between the end pins.

d Solder the center of the BNC connector to the center pin of one row on the Berg strip.

e Solder the ground tab of the BNC connector to the center pin of the other row on the Berg strip.

f On one of the test connectors, solder a 20:1 probe. The probe ground goes to the same row of pins on the test connector as the BNC ground tab.



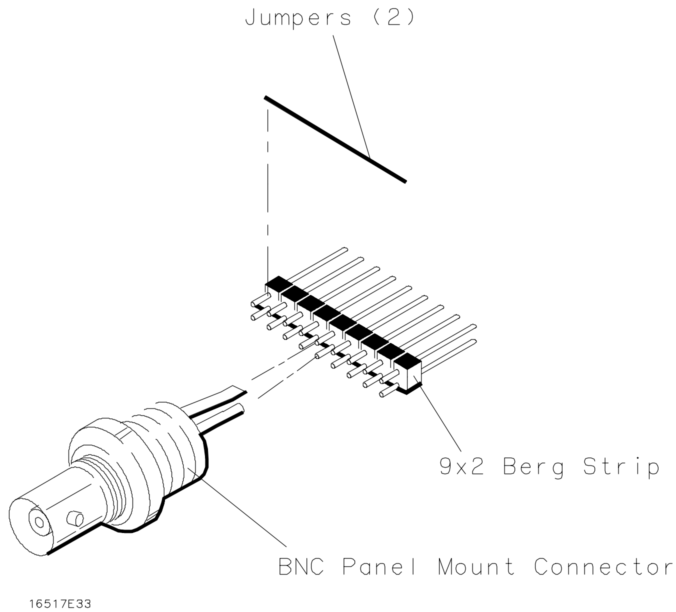
2 Build one test connector using a BNC connector and a 9-by-2 section of Berg strip.

a Solder a jumper wire to all pins on one side of the Berg strip.

b Solder a jumper wire to all pins on the other side of the Berg strip.

c Solder the center of the BNC connector to the center pin of one row on the Berg strip.

d Solder the ground tab of the BNC connector to the center pin of the other row on the Berg strip.



To test the calibration signal

Although the calibration signal test does not test a logic analyzer specification, it does verify the accuracy of the calibration signal. The calibration signal, used for the skew adjustment, is verified using a general purpose 500 MHz oscilloscope. The frequency, rise time, and DC offset voltage are measured and recorded in the performance test record. After the calibration signal is tested and passed, a skew adjust is performed on the 16517A/18A module.

Equipment Required

Equipment	Critical Specifications	Recommended Agilent Model/Part
Digitizing Oscilloscope	≥ 500 MHz Bandwidth	54520A
Oscilloscope Probe	≥ 500 MHz Bandwidth	10441A
BNC Coax Cable	1 GHz Bandwidth	10503A
Calibration Pod	no substitute	16517-63201

Set up the equipment

1 Turn on the equipment required and the logic analyzer. Let them warm up for 30 minutes before beginning the test.

2 Set up the digitizing oscilloscope.

a Press the HORIZONTAL setup and select Repetitive Acquisition.

b Press the Utility key, then select the Probe Cal menu. Select Probe Cal Channel 1 by pressing the Cal Channel menu key a number of times. Select Start Cal and follow the instructions on the oscilloscope display.

3 Using the BNC coax cable, connect the 16517A Calibration Output port to the Calibration Pod.

4 Connect the master card pod 1 data channels and clock channel to the calibration pod Cal ports.

5 Connect the oscilloscope probe tip to one of the unused calibration pod Cal ports. The ground lead can be connected to the ring of the BNC connector.

Capture the calibration signal

1 On the oscilloscope, select Autoscale. Record the pos: (position) voltage in the performance test record as the calibration signal offset voltage.

2 Measure the other signal parameters using the oscilloscope waveform measurement functions.

- **a** Press the oscilloscope Channel 2 On key to turn on channel 2. Select 50 Ω input impedance.
- **b** Select More Preset Probe. Select probe attenuation of 1.000:1.
- **c** Disconnect the BNC coax cable from the calibration pod and connect the cable to the oscilloscope Channel 2 input. Select Autoscale.
- **d** Press the Display key. Select # of averages 16.
- **e** Measure the frequency. Push the blue shift key, then push Frequency, then push 2. The minimum, maximum, and average values should be between 61.875 and 63.125 MHz. Record the value in the performance test record.
- **f** Measure the rise time. Push the blue shift key, then push Rise, then push 2. The minimum, maximum, and average values should be less than 1.35 ns. Record the values in the performance test record.

To perform the self-tests

The self tests verify the correct operation of the module. Self tests can be performed all at once or one at a time. While testing the performance of the module, run the self tests all at once.

If error messages appear during the self tests, refer to chapter 8 for a description of the message.

Loading the PV (performance verification) operating system will overwrite all of the Agilent Technologies 16500-series module configurations. If you would like to keep the configurations, then save the configurations to disk prior to loading the PV system. Refer to the User's Guide for more information on saving configuration files to disk.

Access the self-tests

For an explanation of the tests, refer to the Self-Tests Descriptions in chapter 8.

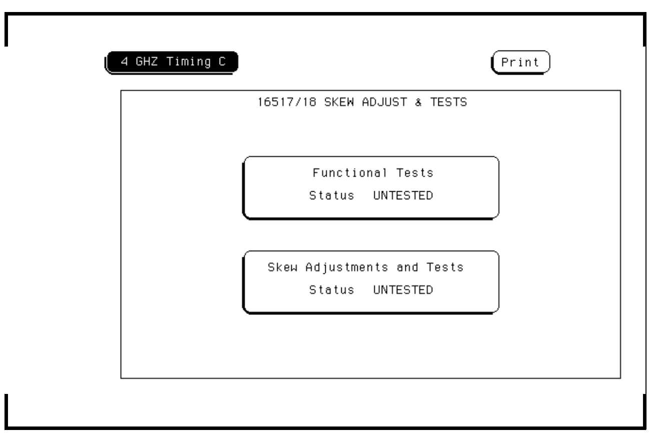
1 Disconnect all inputs, then turn on the power switch if the mainframe is not turned on.

2 In the System Configuration menu, touch Configuration. In the pop-up menu, touch Test.

If the 16517A/18A module is configured in an Agilent Technologies 16500A mainframe, the PV system disk must be installed in one of the flexible disk drives.

3 Touch the box labeled Touch Box to Load Test System.

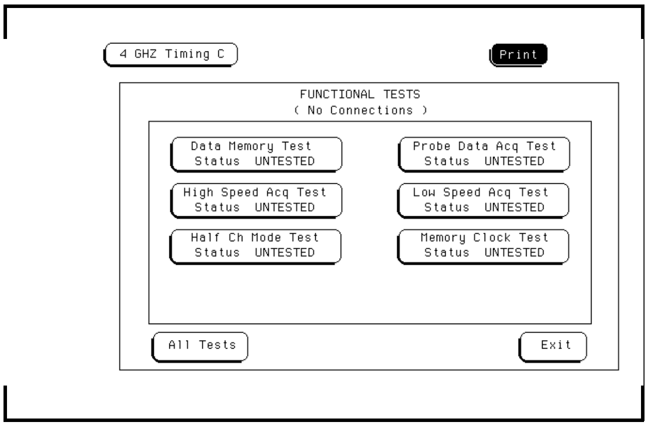
4 On the test system screen, touch Test System. At the pop-up menu, select 4GHz/1GHz LA.



Perform the functional tests

The Functional Tests verify the main subsystems of the 16517A/18A module are functioning. The pod channels are not connected to any type of test signal for any of these tests. If a test fails, a message will appear which indicates which module board failed. Refer to chapter 8 for a description of the error messages.

1 Touch Functional Tests. The functional tests menu appears.



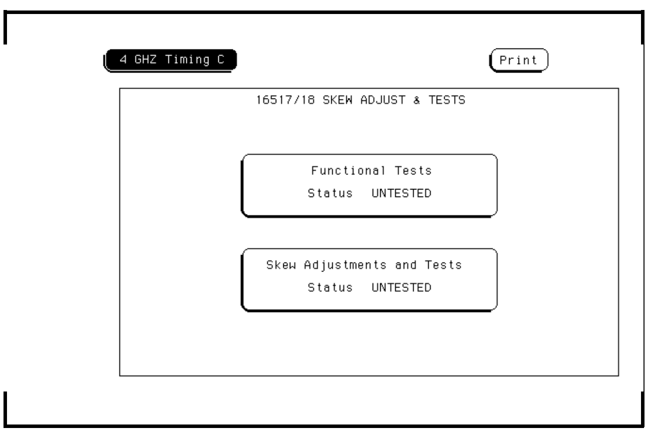
2 To run all of the tests, touch the All Tests field. As each of the functional tests is performed and passed, the status field will change from UNTESTED to PASS.

3 Touch Done to exit the test menu. Touch Exit to exit the Functional Tests menu.

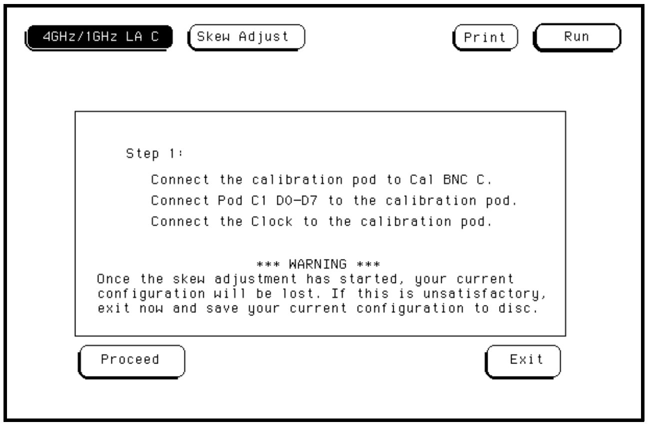
Perform the skew adjustments and tests

Valid skew factors must be present in order to access these tests. The Skew Tests require valid skew factors to ensure that the tests will pass.

1 Touch Skew Adjustments and Tests.



2 Perform the skew adjust procedure. Touch Adjust Clock and Data Path Skew. A BNC coax cable (Agilent Technologies 10503A) and Calibration Pod (16517-63201) are needed. Follow the instructions on the display. At the end of the Skew adjust, save the skew factors to NV-RAM. For more information, refer to "To adjust the channel-to-channel skew" in chapter 4.



3 To run all of the tests, touch the All Tests field. As each of the skew-dependent tests are performed and pass, the status field will change from UNTESTED to PASS.

4 Touch Done to exit the test menu. Touch Exit to exit the Skew Adjustments and Tests menu.

Exit the self-tests

1 Touch the 4GHz/1GHz LA field, then touch Test System.

2 Touch Configuration, then touch Exit Test.

If the 16517A/18A module is configured in an Agilent Technologies 16500A mainframe, the operating system disk must be installed in one of the flexible disk drives.

3 Touch the box labeled Touch box to Exit Test System. The Agilent Technologies 16500 operating system will now load and the system configuration menu will appear.

To test the threshold accuracy

A DC power supply able to change voltage in 1 mV increments is required. The threshold voltage hysteresis is characterized for TTL threshold, ECL threshold, the threshold limits, and for a threshold voltage of 0.00 V for all pods. Testing the threshold accuracy verifies the performance of the following specifications:

- ±(50 mV + 2% of threshold setting)

These instructions include detailed steps for testing the threshold settings of the master card pod 1. After testing the master card pod 1 with all tests through page 3-17, connect and test the rest of the pods one at a time. To test the next pod, follow the detailed steps for master card pod 1, substituting the next pod for master card pod 1 in the instructions.

Each threshold test tells you to record the voltage reading in the performance test record located at the end of this chapter. To check if each test passed, verify that the voltage reading you record is within the limits listed on the performance test record.

Equipment Required

Equipment	Critical Specifications	Recommended Agilent Model/Part
Digital Multimeter	0.1 mV resolution, 0.005% accuracy	3458A
DC Power Supply	1 mV resolution, DC voltage ±5.2 V	3325B Option 002
Ground Clips (8)	no substitute	16517-82105
BNC Cable		10503A
BNC-Banana Cable		11001-60001
BNC Tee		1250-0781
BNC Test Connector, 9 x 2		

Set up the equipment

1 Turn on the equipment required and the logic analysis system mainframe. Let them warm up for 30 minutes if you have not already done so.

2 Set up the function generator.

a Set up the function generator to provide a DC offset voltage at the Main Signal output.

b Disable any AC voltage to the function generator DC output, and enable the high voltage output.

Set up the logic analyzer

1 Select the Acquisition mode field. In the pop-up menu, select State Acquisition Mode: Full Channel.
2 Touch the field showing the channel assignments for master card pod 1. Activate all channels by selecting Clear (if all channels are not activated with asterisks (*) showing in the channel position).
3 Touch the field showing the channel assignments for master card pod 2. Deactivate all channels by selecting Clear. Press Done.

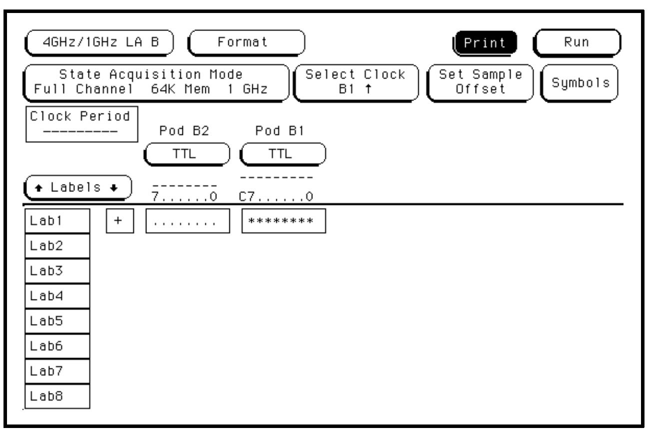
Connect the logic analyzer

1 Using the 9 x 2 test connector, BNC cable, and ground clips, connect the clock and data channels of master card pod 1 to one side of the BNC tee.
2 Using a BNC-banana cable, connect the voltmeter to the other side of the BNC tee.
3 Connect the BNC tee to the Main Signal output of the function generator.

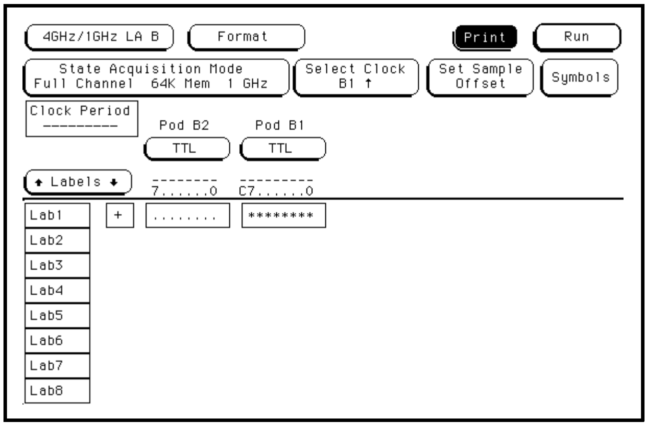
Test the TTL threshold

1 Press the Format key. Select the field below master card pod 1, then select TTL in the pop-up menu.
2 On the function generator front panel, enter 1.595 V ±1 mV DC offset. Use the multimeter to verify the voltage.

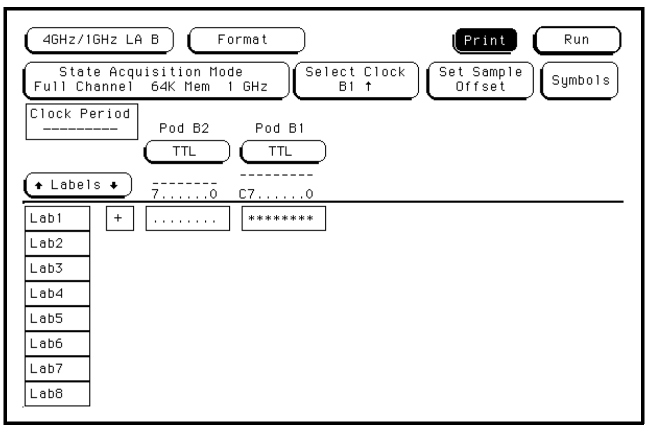
The activity indicators for master card pod 1 should show all data channels and the master card pod 1 clock channel (master board only) at a logic high.



3 Using the Modify down arrow on the function generator, decrease offset voltage in 1 mV increments until all activity indicators for pod 1 show the channels at a logic low. Record the function generator voltage in the performance test record.



4 Using the Modify up arrow on the function generator, increase offset voltage in 1 mV increments until all activity indicators for pod 1 show the channels at a logic high. Record the function generator voltage in the performance test record.



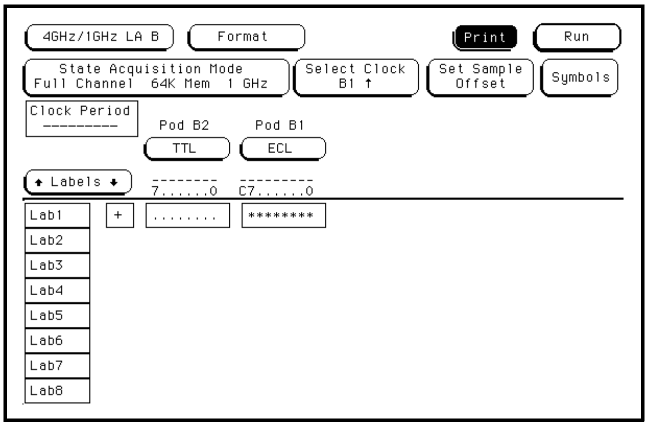
Test the ECL threshold

1 Select the field below master card pod 1, then select ECL in the pop-up menu.

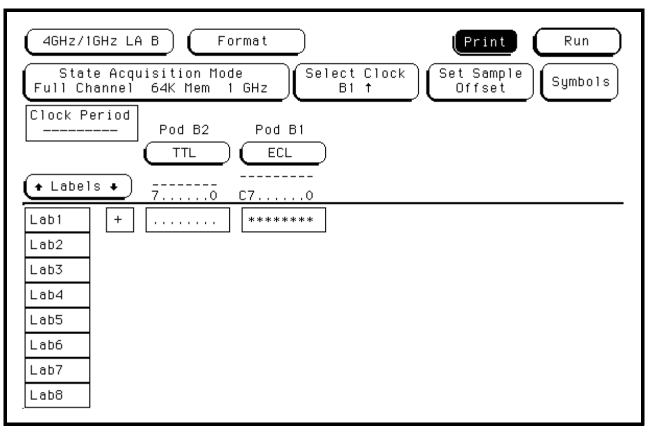
2 On the function generator front panel, enter –1.210 V ±1 mV DC offset. Use the multimeter to verify the voltage.

The activity indicators for pod 1 should show all data channels and the master card pod 1 clock channel (master board only) at a logic high.

3 Using the Modify down arrow on the function generator, decrease offset voltage in 1 mV increments until all activity indicators for pod 1 show the channels are at a logic low. Record the function generator voltage in the performance test record.



4 Using the Modify up arrow on the function generator, increase offset voltage in 1 mV increments until all activity indicators for pod 1 show the channels are at a logic high. Record the function generator voltage in the performance test record.



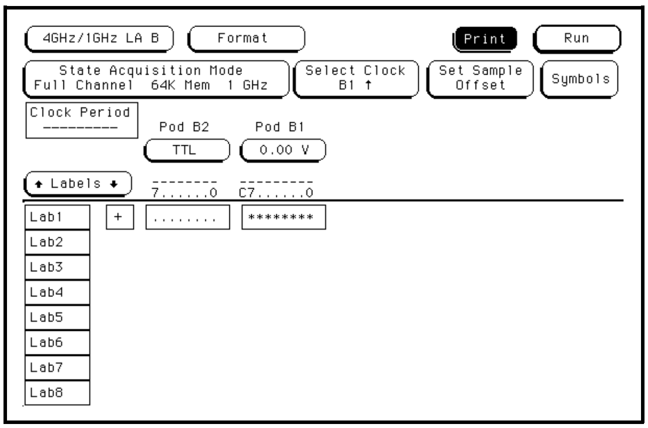
Test the 0 V user-defined threshold

1 Select the field below master card pod 1, then select User in the pop-up menu. At the numeric pop-up menu, enter 0 V.

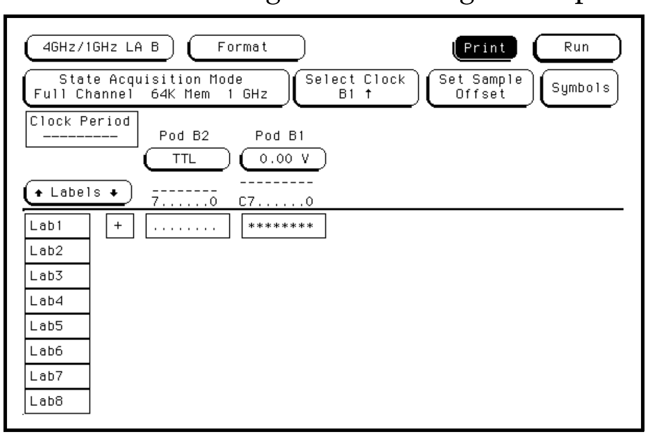
2 On the function generator front panel, enter +0.065 V ±1 mV DC offset. Use the multimeter to verify the voltage.

The activity indicators for pod 1 should show all data channels and the master card pod 1 clock channel (master board only) at a logic high.

3 Using the Modify down arrow on the function generator, decrease offset voltage in 1 mV increments until all activity indicators for pod 1 show the channels at a logic low. Record the function generator voltage in the performance test record.



4 Using the Modify up arrow on the function generator, increase offset voltage in 1 mV increments until all activity indicators for pod 1 show the channels at a logic high. Record the function generator voltage in the performance test record.



Test the next pod

1 Using the 9 x 2 BNC test connector, connect the data channels of the next pod to the output of the function generator until all pods on the master card and expander cards have been tested.

To unassign a pod and assign the next pod to be tested, select the pod, then select Clear in the pop-up menu.

2 Start with "Test the TTL threshold" on page 3–10, substituting the next pod to be tested for master card pod 1.

To test the minimum input voltage swing

The minimum input voltage swing is the smallest voltage amplitude a data signal can have in which the data signal is still recognizable by the logic analyzer. Using a pulse generator, the minimum voltage swing is characterized. Because the actual threshold voltage of a logic analyzer pod can be some value within the threshold specifications, the threshold voltage is characterized as well. Testing the minimum input voltage swing verifies the performance of the following specification:

- 500 mV peak-to-peak

These instructions include detailed steps for testing the minimum input voltage swing of the master card pod 1. After testing the master card pod 1, connect and test the rest of the pods one at a time. To test the next pod, follow the procedure for master card pod 1, substituting the next pod for master card pod 1 in the instructions.

Each test tells you to record the voltage reading in the performance test record located at the end of this chapter. To check if each test passed, verify that the voltage reading you record is within the limits listed on the performance test record.

Equipment Required

Equipment	Critical Specifications	Recommended Agilent Model/Part
Pulse Generator	100 MHz frequency, < 600 ps rise time	8131A
Oscilloscope	> 6 GHz bandwidth	54121T
SMA Coax Cable (2)	18 GHz bandwidth	8120-4948
Adapter	SMA(m) - BNC(f)	1250-1200
Adapter	BNC(m) - BNC(m)	1250-0216
BNC Test Connector, 6 x 2 (quantity 2)	no substitute	
Ground Clips (8)	no substitute	16517-82105

Set up the equipment

1 **Turn on the equipment required and the logic analysis system mainframe. Let them warm up for 30 minutes if you have not already done so.**
2 Set up the pulse generator according to the following table (next page):

Channel 1	**Period**
Delay: 0.0 ps	10.0 ns
DCYC: 50%	
Amplitude: 0.50 V	
Offset: –1.3 V	

Set up the logic analyzer

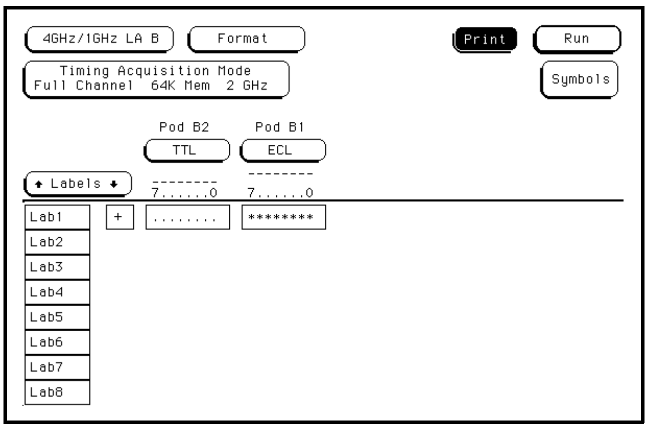
1 Set up the Format menu.

a Select the Acquisition mode field. In the pop-up menu, select Timing Acquisition Mode: Full Channel.

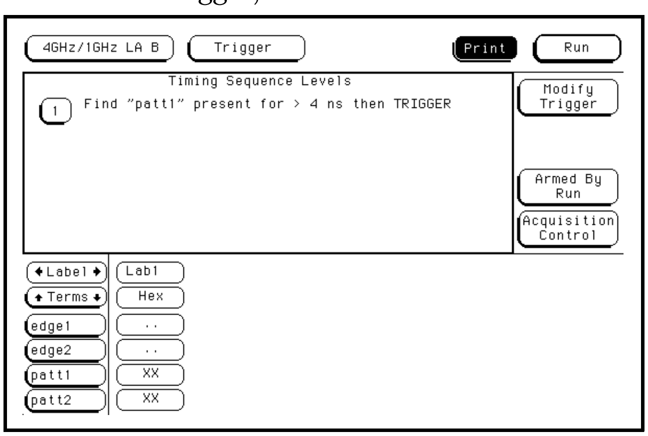
b Touch the field showing the channel assignments for master card pod 1. Activate all channels by selecting Clear (if all channels are not activated with an asterisk (*) showing in the channel position).

c Touch the field showing the channel assignments for master card pod 2. Deactivate all channels by selecting Clear. Press Done.

d Touch the field below master card pod 1, then select ECL in the pop-up menu.



2 Touch Format, then select Trigger. In the Trigger menu, touch Modify Trigger, then select Clear Trigger, then select Clear All.



3 Select Trigger, then touch Waveform. Select the sec/div field. At the numeric pop-up menu, type in 50 ns.

Connect the logic analyzer

1 Using the 6 x 2 test connectors and BNC adapters, connect the data channels of master card pod 1 to the pulse generator output.

a Using one 6 x 2 connector, BNC(m) - BNC(m) adapter, SMA(m) - BNC(f) adapter, and four ground clips, connect data channels 0 - 3 to the pulse generator channel 1 OUTPUT.

b Using one 6 x 2 connector, BNC(m) - BNC(m) adapter, SMA(m) - BNC(f) adapter, and four ground clips, connect data channels 4 - 7 to the pulse generator channel 1 $\overline{\text{OUTPUT}}$.

Connect the oscilloscope

1 Using an SMA cable, connect the pulse generator trigger output to the oscilloscope trigger input.

2 Using an SMA cable, connect the oscilloscope channel 1 input to the Agilent Technologies 54006A probe soldered to one of the BNC test connectors.

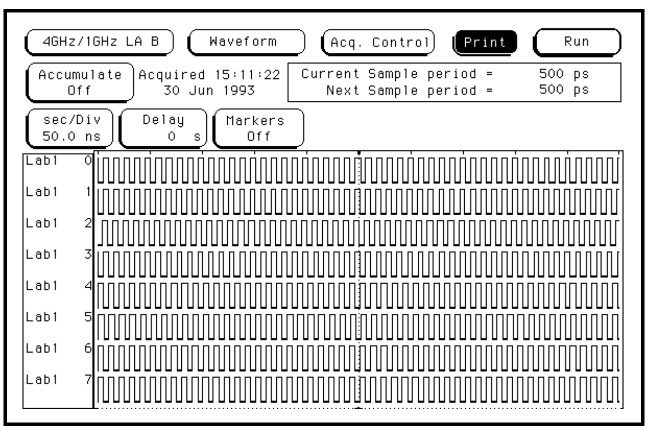
3 Set up the oscilloscope channel 1 menu.

a Press the Channels key on the bottom row of menu keys. Push the channel select key on the vertical row of keys until channel 1 appears.

b Push the PROBE ATTEN key. Select a Ch1 Atten factor of 20.00.

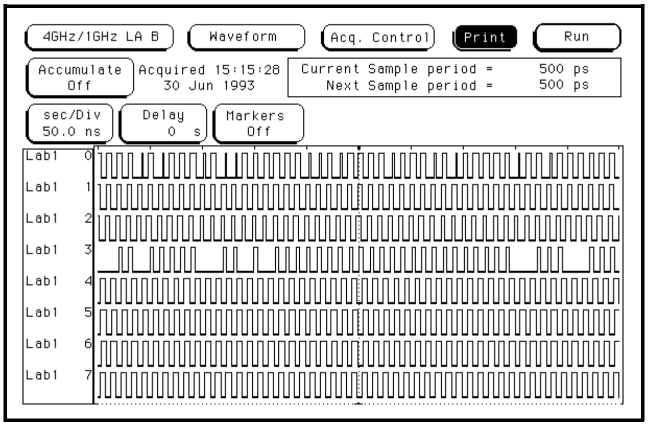
Acquire and verify the data

1 On the 16517A module, select Run-Repetitive. The screen should look similar to that shown below.



If the display looks similar to the one below step 2 (next page), then adjust the pulse generator offset between –1.23 and –1.37 volts until missing pulses are restored. If missing pulses cannot be restored by adjusting the pulse generator offset in this voltage range, this is a failure of this test, and the pod assembly is suspect.

2 On the pulse generator, reduce the channel 1 pulse amplitude in 10 mV steps until missing pulses begin to appear, similar to that shown below.



3 Make a note of the pulse generator offset voltage. Then, on the pulse generator, adjust the channel 1 offset up and down in 10 mV increments between –1.23 and –1.37 volts until there are no missing pulses and the figure looks similar to that below step 1 (previous page). If missing pulses cannot be restored, go to step 5.

4 Repeat steps 2 and 3 until missing pulses can no longer be restored by adjusting the pulse generator offset.

5 Set up the pulse generator offset to the last offset voltage reading where there were no missing pulses (the voltage noted at beginning of step 3). Missing pulses will still appear until the end of step 6.

6 Increase the pulse generator channel 1 amplitude in 10 mV increments until there are no missing pulses. On the 16517A module, touch Stop to stop the acquisition.

7 On the oscilloscope, press the AUTOSCALE key. Read the threshold and voltage swing values. Record the values in the performance test record.

a Press the OFFSET key and read the offset voltage. Record the offset voltage value in the threshold field in the performance test record.

b Press the More key on the bottom row of menu keys. Press the Measure key. Ensure Measure Chan 1 appears at the top of the vertical row of keys. If Measure Chan 1 does not appear, press the key until it does appear.

c Press the More key on the vertical row of keys until Peak-to-Peak Voltage appears at the top of the vertical row of menu keys. Press the Peak-to-Peak Voltage key. Record the Delta-V value at the bottom of the oscilloscope display in the voltage swing fields in the performance test record.

Test the next pod

Beginning with the procedure on page 3-19, "Set up the logic analyzer," continue the test for the rest of the pods, substituting the pod to be tested wherever the test mentions master card pod 1.

To test the minimum clock period

The Minimum Clock Period test utilizes the Agilent Technologies 8131A pulse generator in 1 GHz transducer mode to supply the 16517A master board clock channel with a 1 GHz signal. If the 16517A clock pipeline recognizes the 1 GHz signal then there is confidence that the module will operate as expected with a 1 ns minimum clock period. The clock signal is being properly routed and all the components in the clock pipeline are acknowledging the 1 ns clock signal. This procedure verifies the performance of the following specification:

- Minimum Clock Period: 1.0 ns

Equipment Required

Equipment	Critical Specifications	Recommended Agilent Model/Part
Pulse Generator	1GHz frequency, <600 ps rise time	8131A Option 020
Signal Generator	1GHz frequency	8657A
Adapter	SMA(m) - Probe Tip	16517-27601

Set up the equipment

1 Turn on the equipment required and the Logic Analysis System mainframe. Let them warm up for 30 minutes if you have not already done so.

2 Set up the pulse generator according to the following table:

Pulse Generator Setup

Channel 1	Mode	Ext Input
Delay 0.0 ps Width 500 ps Ampl: 0.80V Offs: -1.3V	TRANS	Thre: 0.5 V

3 Set up the signal generator according to the following table:

Signal Generator Setup

Frequency	Amptd	Modulation
1 GHz	+1.0V	OFF

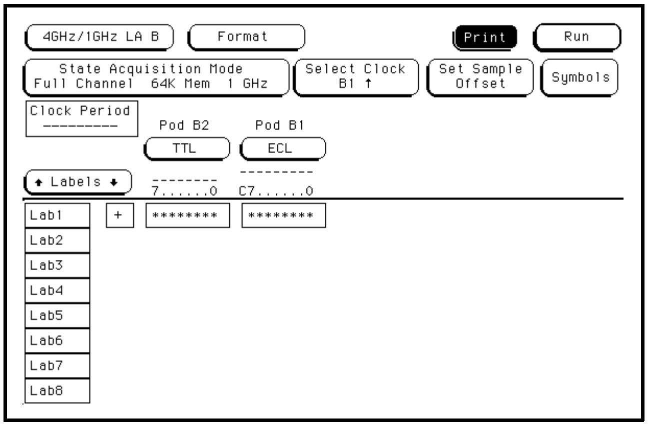
Set up the logic analyzer

1 Set up the Format menu.

a In the Format menu, select State Acquisition Mode Full Channel.

b Touch the threshold field under master pod 1 and select ECL.

c Touch the clock selection field. Select the clock rising edge.



2 Touch Format, then select Trigger. In the Trigger menu, touch Modify Trigger, then select Clear Trigger, then select Clear All.

Check the clock frequency

1 Using the SMA(m) - probe tip adapter, connect the master card pod 1 Clock channel to the pulse generator channel 1 OUTPUT.

2 Activate the pulse generator channel 1 OUTPUT.

3 On the 16517A/18A module, select Trigger, then select Format. The activity indicator should show activity on the master card pod 1 clock channel. If the Clock Period field changes from "-------" and indicates a sample period of 1.000 ns, record a PASS status in the performance test record.

4 In the Format menu, touch the clock selection field. Select the falling clock edge. If the Clock Period field indicates a sample period of 1.000 ns, record a PASS status in the performance test record.

To test pod setup/hold time

The pod setup/hold time test makes use of the sample offset, oversampling, and the state listing compare features of the 16517A/18A module. An Agilent Technologies 8131A in 1 GHz transducer mode is used to supply a signal with 1.400 ns period to the 16517A module through the calibration pod. The sample offset feature positions the actual sample point such that the test data is stable for 350 ps prior to sampling, and also 350 ps after sampling. Because the relationship between the clock signal entering the pod and the sample clock controlling data acquisition is not characterized for oversampling modes, the test may not pass at a 350 ps sample offset. Consequently, the sample point is adjusted until the correct sample offset value is found.

This procedure verifies the performance of the following specification:

- Setup/Hold Time: 400ps/400ps

Equipment Required

Equipment	Critical Specifications	Recommended Agilent Model/Part
Pulse Generator	1GHz frequency, <600 ps rise time	8131A Option 020 *
Signal Generator	1GHz frequency	8657A
Oscilloscope	>6 GHz bandwidth	54121T
Adapter	SMA(f) - BNC(m)	1250-2015
Adapter	BNC(m) - BNC(m)	1250-0216
SMA Cable (3)	18 GHz Bandwidth	8120-4948
BNC Test Connector, 6 x 2 (quantity 2)	no substitute	
Ground Clips (8)	no substitute	16517-82105
Probe		54006A

Set up the equipment

1 Turn on the equipment required and the Logic Analysis System mainframe. Let them warm up for 30 minutes if you have not already done so.

2 Set up the pulse generator according to the following table:

Pulse Generator Setup

Channel 1	Channel 2	Mode	Ext Input
Delay 0.0 ps Width 500 ps Ampl: 0.80V Offs: –1.3V	Delay 0.0 ps Width 500 ps Ampl: 0.80V Offs: –1.3V	TRANS	Thre: 0.5 V

3 Set up the signal generator according to the following table:

Signal Generator Setup

Frequency	Amptd	Modulation
714.285 MHz	+1.0V	OFF

4 Set up the oscilloscope according to the following table:

Oscilloscope Setup

Channel 1	Timebase	Trigger	Display
Display On V/Div 320mV/Div Offset: –1.300 V Probe Atten 20.00	Time/Div 1ns/Div	Trigger Level: –1.000V Probe Atten 1.000	Display Mode Averaged # of Averages 8 Screen Dual Bandwidth 20 GHz

Set up the logic analyzer

1 Set up the Format menu.

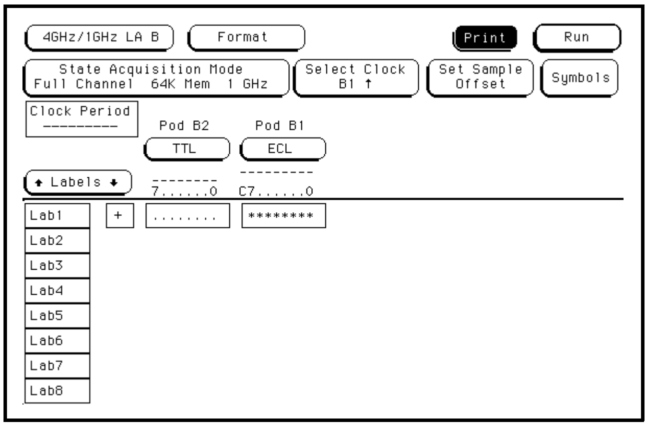
a In the Format menu, select State Acquisition Mode Full Channel.

b Touch the threshold field under master card pod 1. At the pop-up menu, select ECL.

c Touch the field showing the channel assignments for master card pod 1. Touch Clear until all channels are activated (all asterisks), then touch Done.

d Deactivate the channels of the other pods. Touch the field showing the channel assignments for each of the remaining pods. Touch Clear until all channels are deactivated (all periods). Touch Done.

e Touch the clock selection field. Select the clock rising edge.



2 Touch Format, then select Trigger. In the Trigger menu, touch Modify Trigger, then select Clear Trigger, then select Clear All.

Connect the logic analyzer

1 Using the 6 x 2 test connectors and the BNC adapters, connect the data and clock channels of master card pod 1 to the pulse generator channel 1 OUTPUT.

a Using one 6 x 2 connector, BNC(m) - BNC(m) adapter, SMA(m) - BNC(f) adapter, and four ground clips, connect data channels 0 - 3 and the clock channel to the pulse generator channel 1 OUTPUT.

b Using one 6 x 2 connector, BNC(m) - BNC(m) adapter, SMA(m) - BNC(f) adapter, and four ground clips, connect data channels 4 - 7 the pulse generator channel 1 $\overline{\text{OUTPUT}}$.

2 Using an SMA coax cable, connect the oscilloscope channel 1 input to the Agilent Technologies 54006A probe soldered to one of the BNC test connectors.

3 Using an SMA cable, connect the oscilloscope trigger input to the pulse generator channel 2 OUTPUT.

4 Activate the pulse generator channel 1 OUTPUT and channel 2 OUTPUT. The oscilloscope should trigger and the signals from the pulse generator channel 1 outputs should appear.

5 Increase the pulse generator channel 1 AMPL until the waveform measures at least 800 mV amplitude. Change the pulse generator channel 1 OFFS until the waveform is centered on the oscilloscope display.

Acquire the data

1 Configure the logic analyzer to acquire the data.

a In the Trigger menu, touch Acquisition Control.

b In the Acquisition Control menu, select Samples/Clock. In the pop-up menu, select 2.

c Touch Done.

2 Touch Trigger, then select Format. The activity indicators should show activity on the master card pod 1 data channels and on the master card pod 1 clock channel. See that the Clock Period field indicates a sample period of 1.400 ns.

3 Configure the sample offset to +400 ps.

a Select the Set Sample Offset field. Use the knob to set the sample offset value to 400 ps as shown in the Sample Offset field.

b Touch the Sample Offset Mode Coarse field. The field should toggle to Set Offset Mode Fine. Use the knob to set the sample offset value to 350 ps.

4 Set up the Compare menu.

a Touch Format, then touch Listing.

b Select Run-Single. The display should show alternating F0 and 0F for each state. Touch Stop to halt the acquisition.

> If alternating F0 and 0F does not appear, check the logic analyzer connections and grounding. If alternating F0 and 0F still does not appear, select Run-Repetitive, then use the knob to change the sample offset in 50 ps increments between –100 ps and 900 ps until the correct pattern appears on the display.

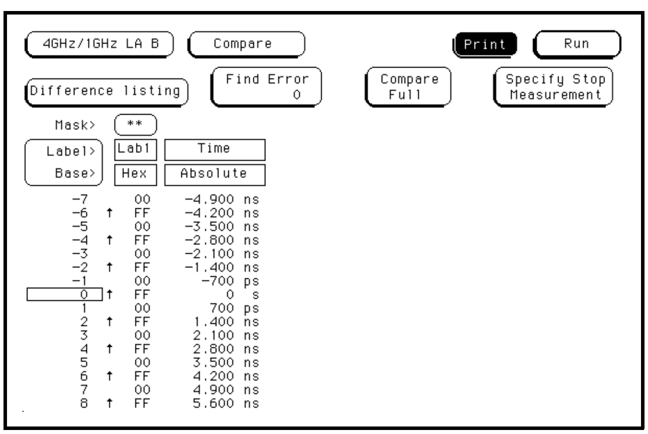
c Touch Listing, then touch Compare. Touch Copy Listing to Reference.

d Touch Specify Stop Measurement. In the pop up menu, touch the Stop Measurement is Off field. In the pop-up menu, select Compare.

e Touch the Equal field. In the pop-up menu, select Not Equal.

f Touch Done.

g Touch the Reference Listing field. The field should toggle to Difference Listing.



5 Test for valid data using the Compare mode. Select Run-Repetitive. If 2 - 4 successive acquisitions are obtained with no failures, then the test passes. Record the pass status in the performance test record; otherwise, repeat steps 4 and 5.

6 Test the next pod.

  a Disconnect the data channels of the pod under test from the calibration module. Do not disconnect the master card pod 1 Clock channel from the calibration pod.

  b Connect the data channels of the next pod to the calibration pod.

  c Repeat the procedure "To acquire the data" for the next pod under test until all pods have been tested.

To test module setup/hold time

The module setup/hold time test makes use of the sample offset, oversampling, and the state listing compare features of the 16517A/18A module. An Agilent Technologies 8131A in 1 GHz transducer mode is used to supply a signal with 3.000 ns period to the 16517A module through the calibration pod. The sample offset feature positions the actual sample point such that the test data is stable for 750 ps prior to sampling, and also 750 ps after sampling. This procedure verifies the performance of the following specification:

- Setup/Hold Time: 750ps/750ps

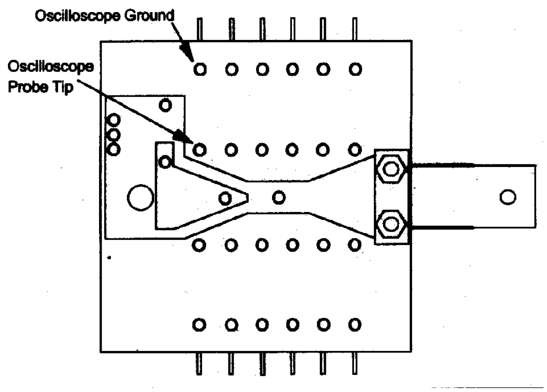
Equipment Required

Equipment	Critical Specifications	Recommended Agilent Model/Part
Pulse Generator	1 GHz frequency, < 600 ps rise time	8131A Option 020
Signal Generator	1GHz frequency	8657A
Adapter, SMA(f) - BNC(m)		1250-2015
SMA Cable (3)	18 GHz Bandwidth	8120-4948
Calibration Module	no substitute	16517-63201
Probe		54006A

Modify the calibration pod

1 Using a Torx 10 screwdriver, remove three screws from the underside of the calibration pod. Then separate the clamshell cover of the calibration pod to remove the calibration pod circuit board.

2 Using a soldering iron, solder the probe tip of the oscilloscope probe to the pad of the signals side of one of the probe connections on the calibration circuit board. Solder the ground to the ground side of the probe connection.



Set up the equipment

1 Turn on the equipment required and the Logic Analysis System mainframe. Let them warm up for 30 minutes if you have not already done so.
2 Set up the pulse generator according to the following table:

Pulse Generator Setup

Channel 1	Channel 2	Mode	Ext Input
Delay 0.0 ps Width 500 ps Ampl: 0.80V Offs: –1.3V	Delay 0.0 ps Width 500 ps Ampl: 0.80V Offs: –1.3V	TRANS	Thre: 0.5 V

3 Set up the signal generator according to the following table:

Signal Generator Setup

Frequency	Amptd	Modulation
333.33 MHz	+1.0V	OFF

4 Set up the oscilloscope according to the following table:

Oscilloscope Setup

Channel 1	Timebase	Trigger	Display
Display On V/Div 320mV/Div Offset: –1.300 V Probe Atten 20.00	Time/Div 1ns/Div	Trigger Level: –1.000V Probe Atten 1.000	Display Mode Averaged # of Averages 8 Screen Dual Bandwidth 20 GHz

Set up the logic analyzer

1 Set up the Format menu.

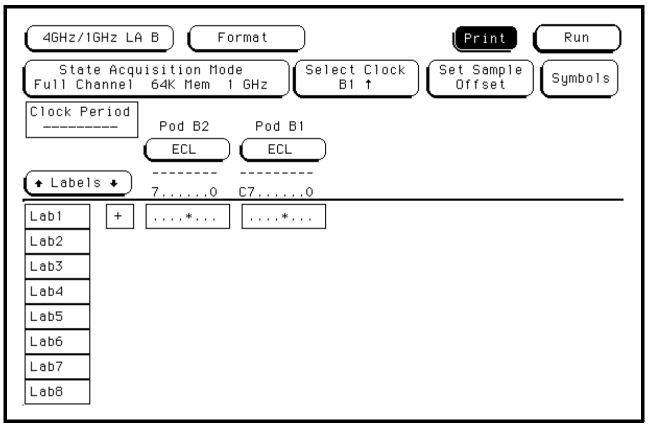
a In the Format menu, select State Acquisition Mode Full Channel.

b Touch the threshold field under each module pod and select ECL.

c Ensure pod channel assignment fields for each pod indicate all channels are deactivated (all periods "."). If any channels are active (showing an asterisk "*" in a channel position) then select that pod channel assignment field. Touch Clear a few times until all pod channel positions are deactivated (all ".") then touch Done.

d Touch the channel assignment field for master card pod 1. Use the knob to scroll the cursor to the channel 3 position. Touch the asterisk field (*) to activate the channel. Repeat for all pods in the module.

e Touch the clock selection field. Select the clock rising edge.



2 Touch Format, then select Trigger. In the Trigger menu, touch Modify Trigger, then select Clear Trigger, then select Clear All.

Connect the logic analyzer

1 Using the modified calibration pod, an SMA coax cable, and SMA(f) - BNC(m) adapter, connect channel 3 of each pod to the pulse generator channel 1 OUTPUT.

2 Plug the master card Clock channel into the calibration pod.

3 Using an SMA cable, connect the oscilloscope trigger input to the pulse generator channel 2 OUTPUT.

4 Activate the pulse generator channel 1 OUTPUT and channel 2 OUTPUT. The oscilloscope should trigger and the signals from the pulse generator channel 1 outputs should appear.

Acquire the data

1 Configure the logic analyzer to acquire the data.

a In the Trigger menu, touch Acquisition Control.

b In the Acquisition Control menu, select Samples/Clock. In the pop-up menu, select 2.

c Touch Done.

2 Touch Trigger, then select Format. The activity indicators should show activity on the master card pod 1 data channels and on the master card pod 1 clock channel. See that the Clock Period field indicates a sample period of 3.000 ns.

3 Configure the sample offset to +750 ps.

a Select the Set Sample Offset field. Use the knob to set the sample offset to 800 ps as shown in the Sample Offset field.

b Touch the Sample Offset Mode Coarse field. The field should toggle to Set Offset Mode Fine. Use the knob to set the sample offset to 750 ps as shown in the Sample Offset field.

4 Set up the Compare menu.

a Touch Format, then touch Listing.

b Select Run-Single. The display should show alternating 0s and 1s for each state.

> The hexadecimal value for the 1s pattern depends on the number of expander cards configured in the module. A master card yields "3" (11), a master card and one expander yields "F" (1111), a master card and two expander yields "3F" (111111), etc.

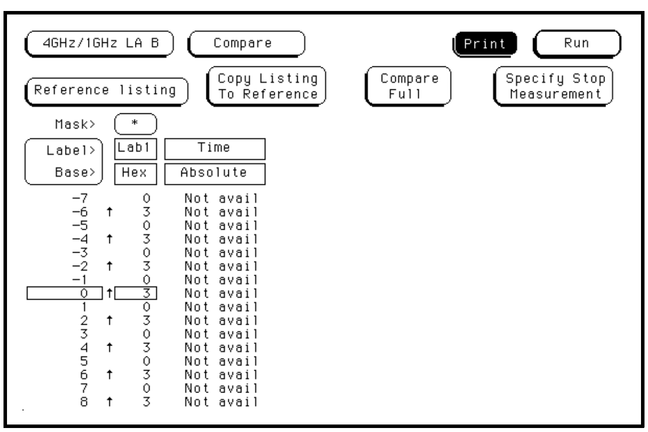
c Touch Listing, then touch Compare. Touch Copy Listing to Reference.

d Touch Specify Stop Measurement. In the pop up menu, touch the Stop Measurement is Off field. In the pop-up menu, select Compare.

e Touch the Equal field. In the pop-up menu, select Not Equal.

f Touch Done.

g Touch the Reference Listing field. The field should toggle to Difference Listing.



5 Test for valid data using the Compare mode.

a Select Run-Repetative. If 2 - 4 successive acquisitions are obtained with no failures, then the test passes. Record the pass status in the performance test record.

b Touch the Find Error field. Use the knob to increment the Find Error numbers. If the white hexadecimal number appearing at every error location is either "0" or "F", then the reference listing is not valid. Proceed to step 6.

c If the white hexadecimal number appearing at every error location is some value other than "F", then the data acquired at this procedure step is not valid. Proceed to step 7.

6 If the reference listing is not valid, perform the following steps:

a Touch the Difference Listing field. The field should toggle to Reference Listing.

b Touch Copy Listing to Reference.

c Touch the Reference Listing field and repeat step 5. A valid reference listing should now be in memory.

7 If the acquired listing is not valid, perform the following steps:

a Verify the signal amplitude, offset and duty cycle using the oscilloscope. Make adjustments as necessary (the duty cycle is changed by varying the external input threshold voltage, EXT INPUT - THRE).

b Repeat step 4. If valid data is not captured, then suspect first the pod, then the circuit board being tested.

To test the time interval accuracy

The time interval accuracy test verifies that the degradation of the frequency of the master oscillator over time does not fall outside of acceptable limits. A test signal is provided by a pulse generator. The 16517A/18A timing mode markers and statistics are used to measure a known time interval. If the time interval value is outside of the limits, then the oscillator has drifted and the logic analyzer module data sampling is not reliable in internal sampling modes. Testing the time interval accuracy does not check a specification, but does check the following:

- 125 MHz oscillator

Equipment Required

Equipment	Critical Specifications	Recommended Agilent Model/Part
Pulse Generator	100 MHz 3.5 ns pulse width, < 600 ps rise time	8131A Option 020
Function Generator	Accuracy $\leq (5)(10^{-6}) \times$ frequency	3325B Option 002
SMA Cable		8120-4948
Adapter	SMA-probe cable	16517-27601
Adapter	BNC(m)-SMA(f)	1250-2015

Set up the equipment

1 Turn on the equipment required and the logic analyzer. Let them warm up for 30 minutes if you have not already done so.

2 Set up the pulse generator according to the following table:

Pulse Generator Setup

Channel 1	Period	Mode	EXT TRIG
Delay: 0 ps	50 ns	TRIG	Slope: Positive
Width: 25 ns			THRE: 1.0 V
High: –0.9 V			
Low: –1.7 V			
COMP: Disabled (LED off)			

3 Set up the function generator according to the following table:

Function Generator Setup

Freq: 20 000 000 . 0 Hz	Main Function: Sine wave
Amplitude: 3.000 V	High Voltage: Disabled (LED Off)
Phase: 0.0 deg	
DC Offset: 0.0 V	

Set up the logic analyzer

1 Set up the Format menu.

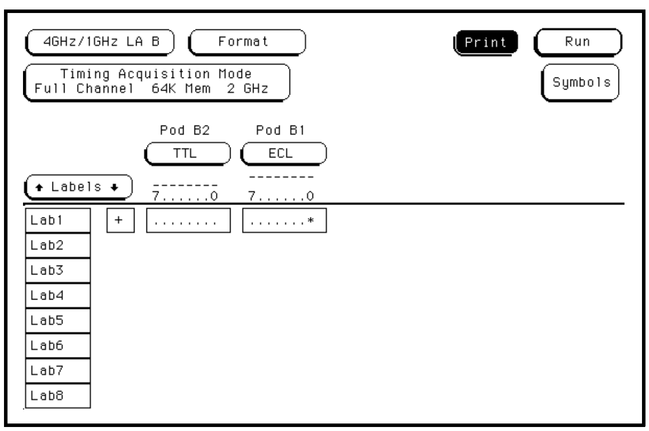
a Touch the field to the right of 4GHz/1GHz LA B, and touch Format in the pop-up menu.

b In the Format menu, touch Timing Acquisition Mode Full Channel.

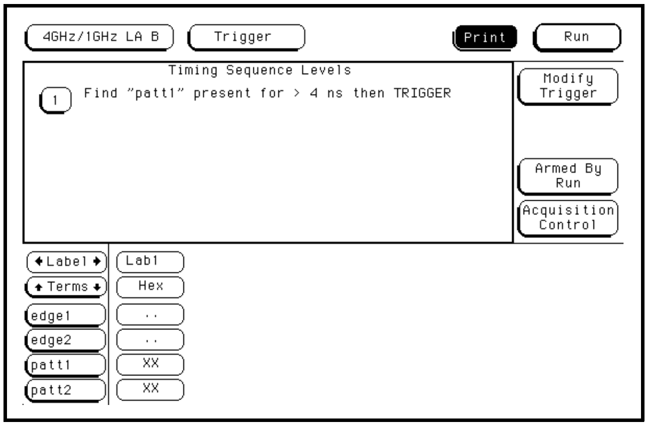
c Touch the threshold field under master card pod 1 and select ECL.

d Touch the field showing the channel assignments for master card pod 1. Deactivate all channels by selecting Clear. Using the knob, move the cursor to channel 0. Touch the asterisk field to put an asterisk in the channel 0 position, activating the channel, then touch Done.

e Touch the field showing the channel assignments for master card pod 2. Deactivate all channels by selecting Clear. Touch Done.



2 Touch Format, then select Trigger. In the Trigger menu, touch Modify Trigger, then select Clear Trigger, then select Clear All.



3 Set up the Waveform menu.

a Select Trigger, then select Waveform.

b Select Acq Control. In the pop-up menu, select Sample Period. In the Sample Period pop-up menu, select 8 ns. Select Trigger Position Center. In the Trigger Position pop-up menu, select Start. Select Done to exit the Acq Control menu.

c Select the sec/Div field. In the pop-up menu, type 50.0 ns, then select Done.

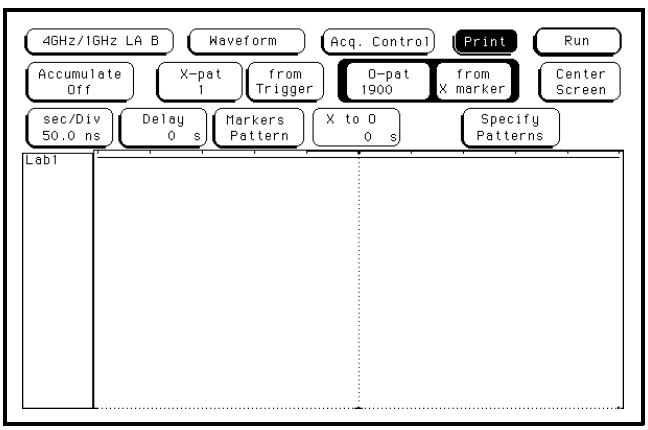
d Select the Markers Off field, then select Pattern.

e Select the Specify Patterns field. Select X entering 1 and O entering 1. Select Done to exit the Specify Patterns menu.

f Select the X-pat field. Type "1," then select Done.

g Select the O-pat field. Type "1900," then select Done.

h Select the O-pat from trigger field, then select from X-marker.



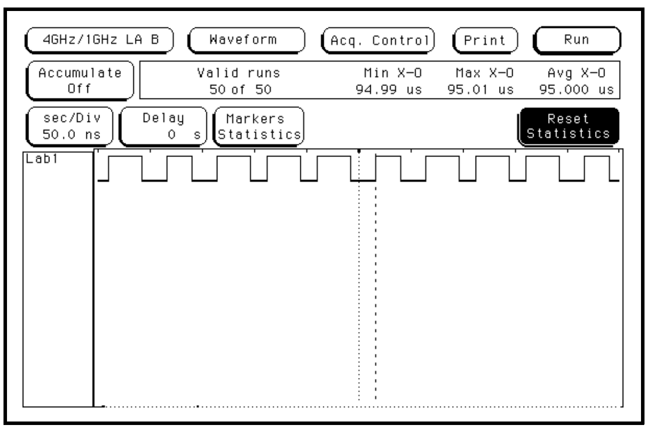
i Select the Markers Patterns field, then select Statistics. Select Reset Statistics to initialize the statistics fields.

Connect the logic analyzer

1 Using a SMA - probe cable adapter, connect channel 0 of Pod 1 to the pulse generator channel 1 output.
2 Using the SMA cable and the BNC(m) - SMA(f) adapter, connect the External Input of the pulse generator to the Main Signal output of the function generator.

Acquire the data

1 Enable the pulse generator channel 1 output (with the LED off).
2 Select Run-Repetitive. Allow the logic analyzer to acquire data for at least 50 valid runs as indicated in the pattern statistics field.
3 When the logic analyzer has acquired at least 50 valid runs, touch Stop. The Min X-O field in the logic analyzer Pattern Statistics menu should read 94.99–95.00 µs. The Max X-O field should read 95.00–95.01 µs. The Avg X-O field should read 94.99–95.01 µs. Record the results in the performance test record.



Performance Test Record

Performance Test Record

	Agilent Technologies 16517A/18A Logic Analyzer_______
Serial No.______________________	Work Order No.___________________
Recommended Test Interval - 2 Year/4000 hours	Date___________________
Recommended next testing___________________	Temperature___________________

Test	Settings	Results		
Calibration Signal	DC Offset Voltage		_________	
	Frequency	61.875 - 63.125 MHz	_________	
	Rise Time	< 1.35 ns	_________	
Self-Tests		Pass/Fail	_________	
Deskew Procedure		Performed/Not Performed	_________	
Threshold Accuracy Master Card, Pod 1	TTL	4.850 - 5.150 V	_________	_________
	ECL	–1.376 - –1.224 V	_________	_________
	–5.00 V User	–5.150 - –4.850 V	_________	_________
	+5.00 V User	5.150 - 4.850 V	_________	_________
	0 V User•	–0.050 - 0.050	_________	_________
Master Card, Pod 2	TTL	4.850 - 5.150 V	_________	_________
	ECL	–1.376 - –1.224 V	_________	_________
	–5.00 V User	–5.150 - –4.850 V	_________	_________
	+5.00 V User	5.150 - 4.850 V	_________	_________
	0 V User•	–0.050 - 0.050	_________	_________
Exp. Card 1, Pod 1	TTL	4.850 - 5.150 V	_________	_________
	ECL	–1.376 - –1.224 V	_________	_________
	–5.00 V User	–5.150 - –4.850 V	_________	_________
	+5.00 V User	5.150 - 4.850 V	_________	_________
	0 V User•	–0.050 - 0.050	_________	_________
Exp. Card 2, Pod 2	TTL	4.850 - 5.150 V	_________	_________
	ECL	–1.376 - –1.224 V	_________	_________
	–5.00 V User	–5.150 - –4.850 V	_________	_________
	+5.00 V User	5.150 - 4.850 V	_________	_________
	0 V User•	–0.050 - 0.050	_________	_________

Performance Test Record

Test	Settings	Results		
Exp. Card 2, Pod 1	TTL	4.850 - 5.150 V	________	________
	ECL	–1.376 - –1.224 V	________	________
	–5.00 V User	–5.150 - –4.850 V	________	________
	+5.00 V User	5.150 - 4.850 V	________	________
	0 V User•	–0.050 - 0.050	________	________
Exp. Card 2, Pod 2	TTL	4.850 - 5.150 V	________	________
	ECL	–1.376 - –1.224 V	________	________
	–5.00 V User	–5.150 - –4.850 V	________	________
	+5.00 V User	5.150 - 4.850 V	________	________
	0 V User•	–0.050 - 0.050	________	________
Exp. Card 3, Pod 1	TTL	4.850 - 5.150 V	________	________
	ECL	–1.376 - –1.224 V	________	________
	–5.00 V User	–5.150 - –4.850 V	________	________
	+5.00 V User	5.150 - 4.850 V	________	________
	0 V User•	–0.050 - 0.050	________	________
Exp. Card 3, Pod 2	TTL	4.850 - 5.150 V	________	________
	ECL	–1.376 - –1.224 V	________	________
	–5.00 V User	–5.150 - –4.850 V	________	________
	+5.00 V User	5.150 - 4.850 V	________	________
	0 V User•	–0.050 - 0.050	________	________
Exp. Card 4, Pod 1	TTL	4.850 - 5.150 V	________	________
	ECL	–1.376 - –1.224 V	________	________
	–5.00 V User	–5.150 - –4.850 V	________	________
	+5.00 V User	5.150 - 4.850 V	________	________
	0 V User•	–0.050 - 0.050	________	________
Exp. Card 4, Pod 2	TTL	4.850 - 5.150 V	________	________
	ECL	–1.376 - –1.224 V	________	________
	–5.00 V User	–5.150 - –4.850 V	________	________
	+5.00 V User	5.150 - 4.850 V	________	________
	0 V User•	–0.050 - 0.050	________	________

Test	Settings	Results	
Minimum Input Voltage Swing Master Card Pod 1	Threshold Swing	≤ 500 mV	________ ________
Master Card, Pod 2	Threshold Swing	≤ 500 mV	________ ________
Exp. Card 1, Pod 1	Threshold Swing	≤ 500 mV	________ ________
Exp. Card 1, Pod 2	Threshold Swing	≤ 500 mV	________ ________
Exp. Card 2, Pod 1	Threshold Swing	≤ 500 mV	________ ________
Exp. Card 2, Pod 2	Threshold Swing	≤ 500 mV	________ ________
Exp. Card 3, Pod 1	Threshold Swing	≤ 500 mV	________ ________
Exp. Card 3, Pod 2	Threshold Swing	≤ 500 mV	________ ________
Exp. Card 4, Pod 1	Threshold Swing	≤ 500 mV	________ ________
Exp. Card 4, Pod 2	Threshold Swing	≤ 500 mV	________ ________
Minimum Clock Period	Trigger Falling Clock Edge	Pass/Fail Pass/Fail	________ ________
Pod Setup/Hold Master Card, Pod 1		Pass/Fail	________
Master Card, Pod 2		Pass/Fail	________
Exp. Card 1, Pod 1		Pass/Fail	________
Exp. Card 1, Pod 2		Pass/Fail	________
Exp. Card 2, Pod 1		Pass/Fail	________
Exp. Card 2, Pod 2		Pass/Fail	________

Performance Test Record

Test	Settings	Results

Pod Setup/Hold Exp. Card 3, Pod 1		Pass/Fail	________
Exp. Card 3, Pod 2		Pass/Fail	________
Exp. Card 4, Pod 1		Pass/Fail	________
Exp. Card 4, Pod 2		Pass/Fail	________
Module Setup/Hold		Pass/Fail	________
Time Interval Accuracy	Min X-O Max X-O Avg X-O	94.99 - 95.00 µs 95.00 - 95.01 µs 94.99 - 95.01 µs	________ ________ ________

4

Calibrating and Adjusting

Calibrating and Adjusting

This chapter gives you instructions for calibrating and adjusting the data acquisition module. Though the module specifications are not tested during these procedures, the module must be adjusted to ensure the specifications will be met.

Some modules for the Logic Analysis System require calibration if you move them to a different slot. For calibration information, refer to the manuals for the individual modules.

The adjustment to the data acquisition module consists of skew adjustment to minimize channel-to-channel skew. The adjustment factors are stored in nonvolatile RAM, and are loaded up at system start up.

To periodically verify the performance of the data acquisition module against the module specifications, refer to "Testing Performance" in chapter 3.

To calibrate the data acquisition module

The 16517A/18A does not require an operational accuracy calibration. To test the module against the module specifications, refer to "Testing Performance" in chapter 3.

To adjust the channel-to-channel skew

Equipment Required

Equipment	Critical Specification	Recommended Agilent Model/Part	Qty
Calibration Module	No Substitutes	16517-63201	1
BNC Coax Cable		10503A	1

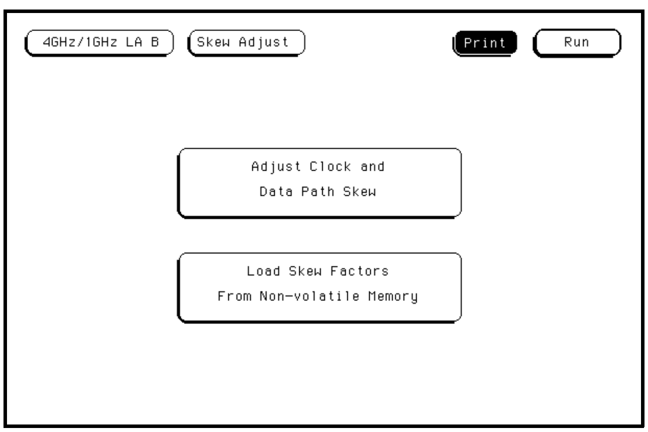
Connect the logic analyzer

1 Connect one end of the BNC cable to the calibration output port on the 16517A master board rear panel.

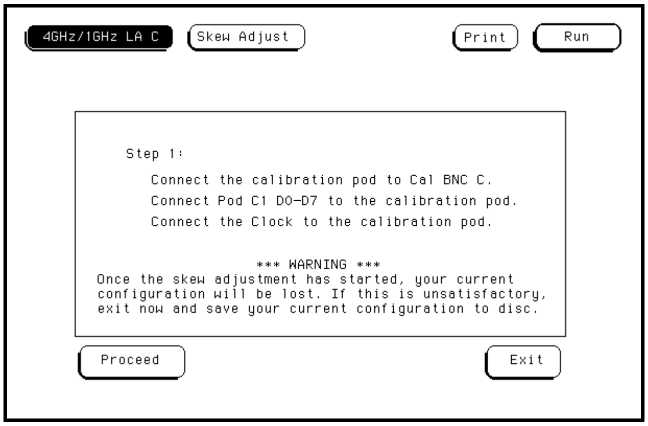
2 Connect the other end of the BNC cable to the BNC Signal Input of the calibration module.

Set up the logic analyzer

1 In the System Configuration menu, touch System, 4GHz/1GHz LA, then touch Format. In the pop-up menu, touch Skew Adjust.



2 In the Skew Adjust menu, touch Perform Clock and Data Path Deskew.

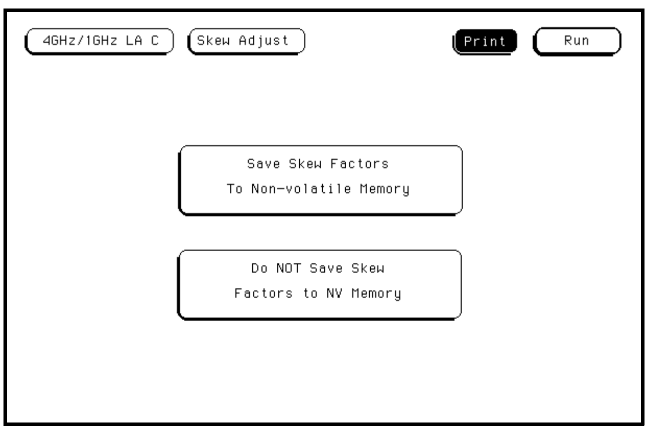


3 Follow the instructions on the screen to connect the pods to the calibration module. After connecting the pod to the calibration module, touch Proceed.

4 Continue following the instructions on the screen to connect the various pods to the calibration module until all pods are skew adjusted.

Save or discard the skew factors

When the skew adjustment is complete, the choice is given to save or not save the skew factors. To not save the skew factors, touch Do Not Save Skew Factors. To save the skew factors, touch Save Skew Factors to NV-RAM.



Exit the skew adjust menu

To exit the skew adjust menu, touch Skew Adjust, then touch Format in the pop-up menu.

5

Troubleshooting

Troubleshooting

This chapter helps you troubleshoot the module to find defective assemblies. The troubleshooting consists of flowcharts, self-test instructions, and a test for the auxiliary power supplied by the probe cable. This information is not intended for component-level repair.

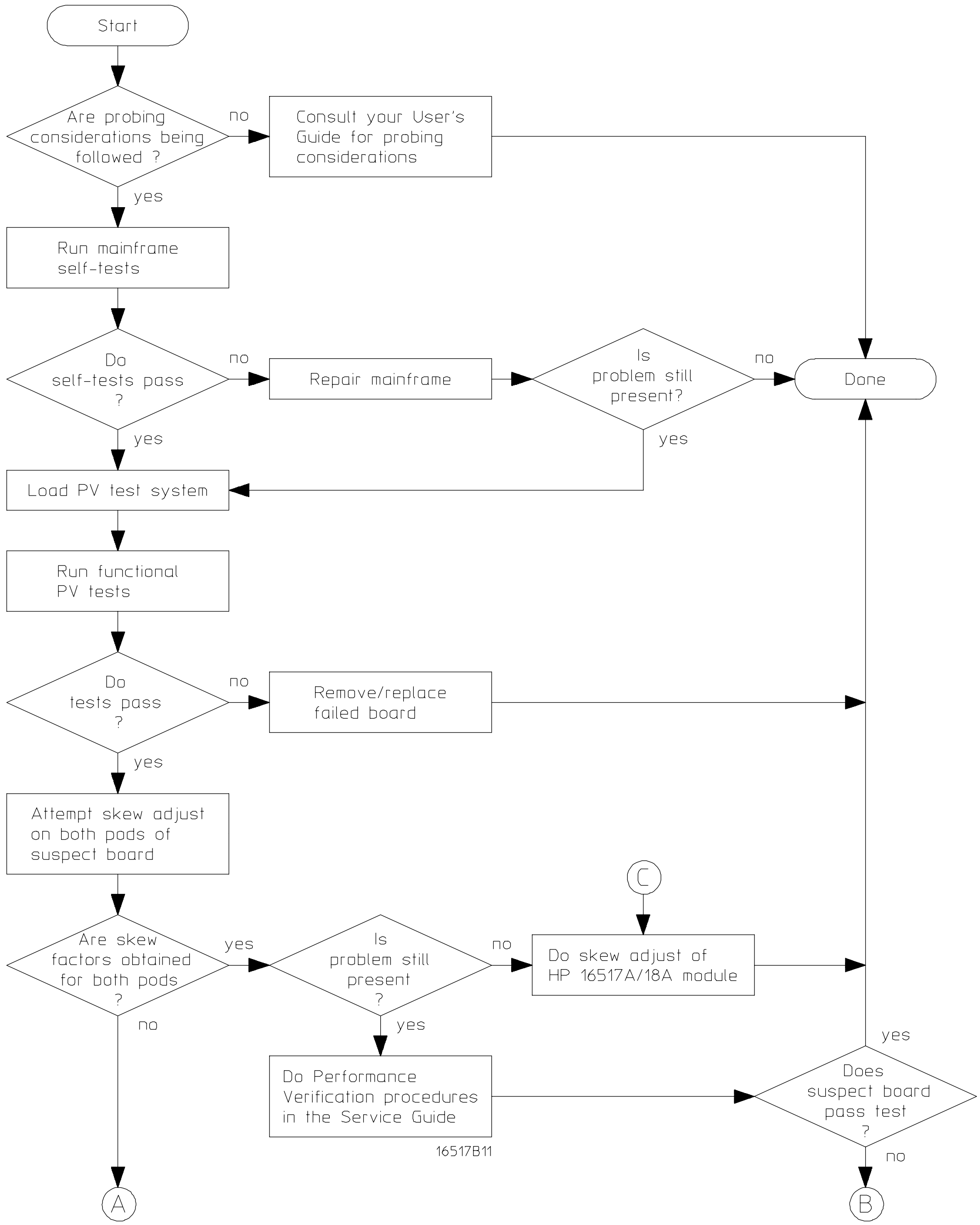
The service strategy for this instrument is the replacement of defective assemblies. This module can be returned to Agilent Technologies for all service work, including troubleshooting. For replacement procedures, refer to chapter 6, "Replacing Assemblies." For the return procedure, refer to "To return assemblies" in chapter 6. Contact your nearest Agilent Technologies Sales Office for more details.

To troubleshoot the analyzer

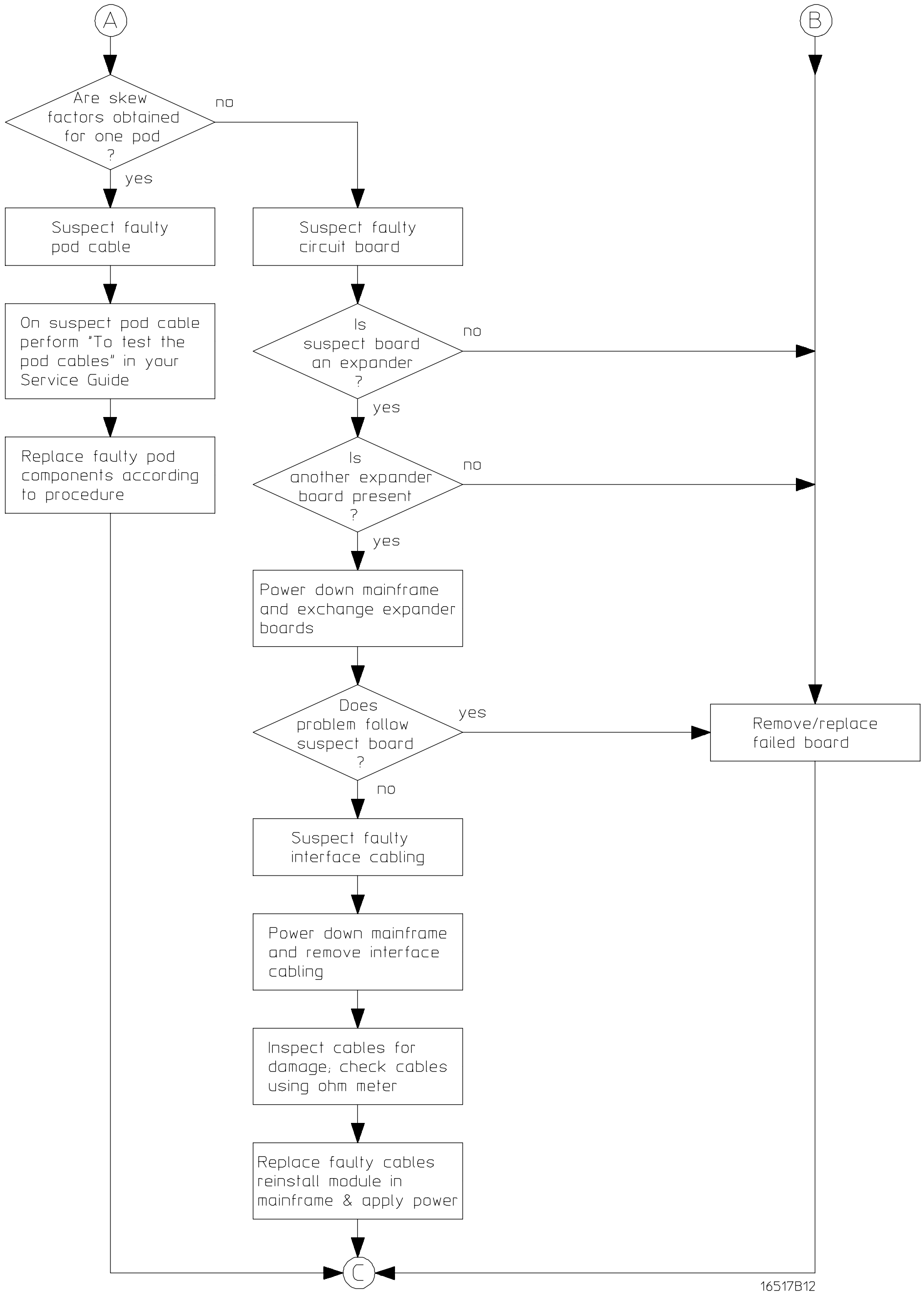
If you suspect a problem, start at the top of the first flowchart. Flowcharts are the primary tool used to isolate defective assemblies. The flowcharts refer to other tests to help isolate the trouble. The circled letters on the charts indicate connections with the other flowcharts. Start your troubleshooting at the top of the first flowchart. During the troubleshooting instructions, the flowcharts will direct you to perform the self-tests.

CAUTION

Electrostatic discharge can damage electronic components. Use grounded wriststraps and mats when you perform any service to this instrument or to the cards in it.



Troubleshooting Flowchart 1



Troubleshooting Flowchart 2

To run the self-tests

Self-tests for the module identify the correct operation of major functional areas of the module. You can run all self-tests without accessing the interior of the instrument. If a self-test fails, the troubleshooting flowcharts instruct you to change a card or cable of the module. The error messages which might appear during self tests are described in chapter 8.

Loading the PV (performance verification) operating system will overwrite all of the Agilent Technologies 16500-series module configurations. If you would like to keep the configurations, then save the configurations to disk prior to loading the PV system. Refer to the User's Guide for more information on saving configuration files to disk.

Access the self-tests

For an explanation of the tests, refer to the Self-Tests Descriptions in chapter 8.

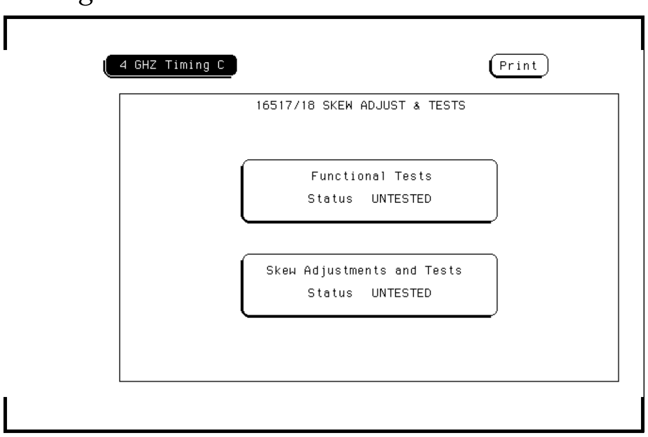
1 Disconnect all inputs, then turn on the power switch if the mainframe is not turned on.

2 In the System Configuration menu, touch Configuration. In the pop-up menu, touch Test.

If the 16517A/18A module is configured in an Agilent Technologies 16500A mainframe, the PV system disk must be installed in one of the flexible disk drives.

3 Touch the box labeled Touch Box to Load Test System.

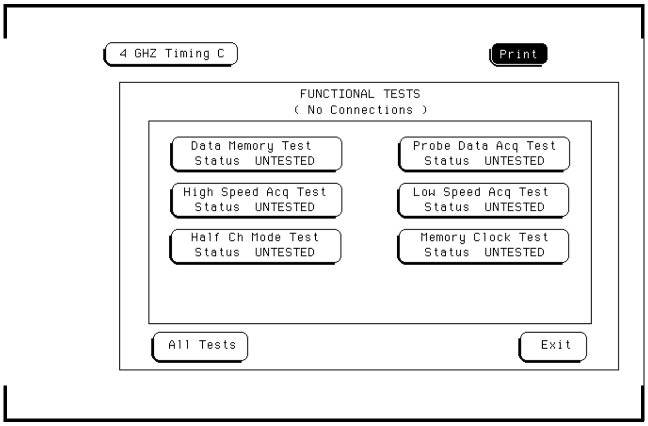
4 On the test system screen, touch Test System. At the pop-up menu, select 4 GHz Timing.



Perform the functional tests

The Functional Tests verify the main subsystems of the 16517A/18A module are functioning. The pod channels are not connected to any type of test signal for any of these tests. If a test fails, a message will appear which indicates which module board failed.

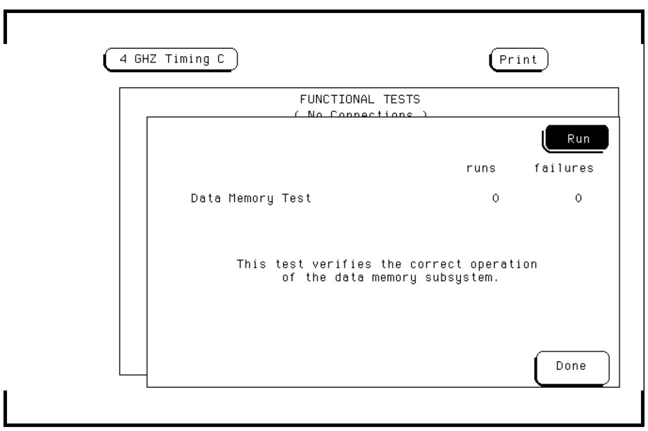
1 Touch Functional Tests. The functional tests menu appears.



2 To run all of the tests, touch the All Tests field. As each of the functional tests is performed and passed, the status field will change from UNTESTED to PASS.

3 If you want to run each test individually, then perform the following steps:

a Select the functional test of interest. For this example, the Data Memory Test will be run. Touch the field labeled Data Memory Test and the Data Memory Test menu will appear.



b Touch Run. After the test is completed, the runs field is increment. If the test fails, then the failures field is increment and a message appears indicating the failed board.

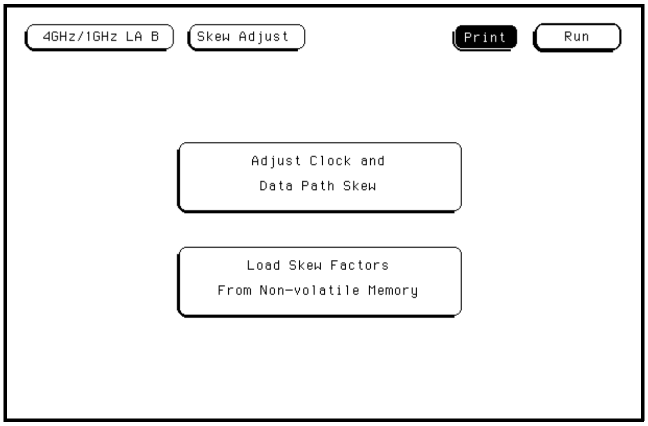
c Touch Done to exit the test menu.

4 Touch Exit to exit the Functional Tests menu.

Perform the skew adjustments and tests

Valid skew factors must be present in order to access these tests. The Skew Tests require valid skew factors to ensure that the tests will pass.

1 Touch Skew Adjustments and Tests.

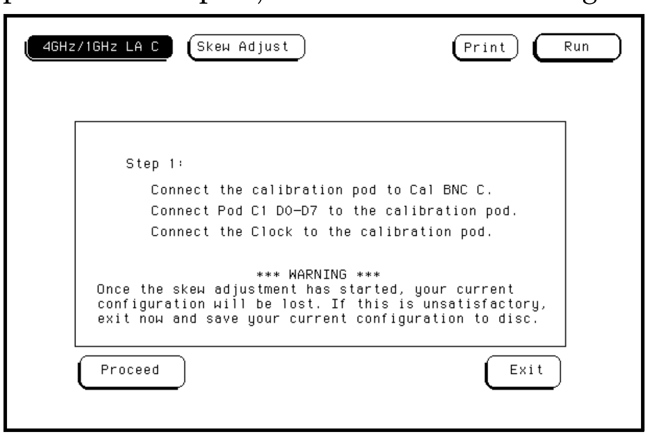


2 Obtain valid skew factors.

a Touch Adjust Clock and Data Path Skew if new skew factors are desired. A BNC coax cable (Agilent Technologies 10503A) calibration pod (16517-63201) are needed. Follow the instructions on the display. For more information, refer to "To adjust the channel-to-channel skew" in Chapter 4.

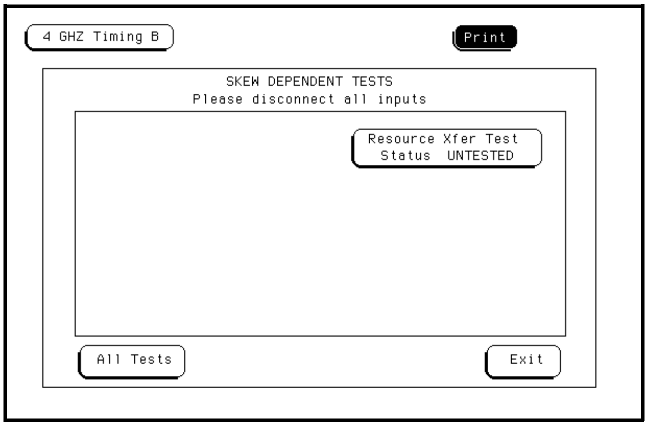
b Touch Load Skew Factors From Non-Volatile Memory if the current skew factors are desired.

3 To run all of the tests, touch the All Tests field. As each of the functional tests are performed and pass, the status field will change from UNTESTED to PASS.



4 If you want to run each test individually, then perform the following steps:

a Select the functional test of interest. For this example, the Resource Xfer Test will be run. Touch the field labeled Resource Xfer Test and the Resource Xfer Test menu will appear.



b Touch Run. After the test is completed, the runs field is increment. If the test fails, then the failures field is incremented and a message appears indicating the failed board.

c Touch Done to exit the test menu.

4 Touch Exit to exit the Skew Adjustments and Tests menu.

Exit the self-tests

1 Touch the 4 GHZ Timing field, then touch Test System.

2 Touch Configuration, then touch Exit Test.

> If the 16517A/18A module is configured in an Agilent Technologies 16500A mainframe, the operating system disk must be installed in one of the flexible disk drives.

3 Touch the box labeled Touch box to Exit Test System. The Agilent Technologies 16500 operating system will now load and the system configuration menu will appear.

To test the pod cables

This test allows you to functionally verify the probe cable and probe tip assembly of any of the logic analyzer pods. Only one probe cable can be tested at a time. Repeat this test for each probe cable to be tested.

CAUTION

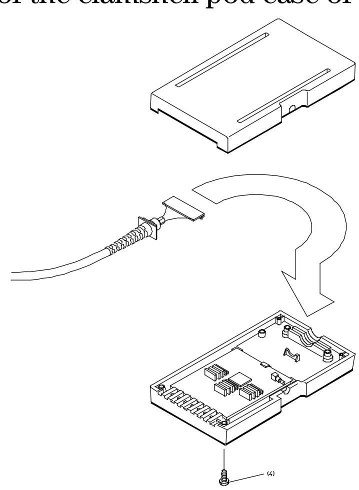
The effects of ELECTROSTATIC DISCHARGE can damage electronic equipment. Use grounded wrist straps and mats when you are performing any kind of service to the pods and pod cables.

Equipment Required

Equipment	Critical Specification	Recommended Agilent Model/Part
Oscilloscope	500 MHz Bandwidth	54520A
Oscilloscope Probe	500 MHz Bandwidth	10441A

Set up the Equipment

1. Remove power from the mainframe.
2. Connect all channels of the suspect pod to the calibration module. Using a BNC cable, connect the calibration pod to the cal port on the rear panel of the 16517A Master Board.
3. Using a Torx 10 screwdriver, remove 4 screws holding the clamshell pod case together. Lift the top off of the clamshell pod case of the pod assembly.



4. Apply power to the mainframe. When the system configuration menu appears, perform the following steps:
   a. Touch System, then select 4GHz/1GHz LA.
   b. In the Format menu, touch the threshold field below the label of the pod under test. At the pop-up menu, select ECL voltage threshold. The activity indicators for the pod under test should show activity.

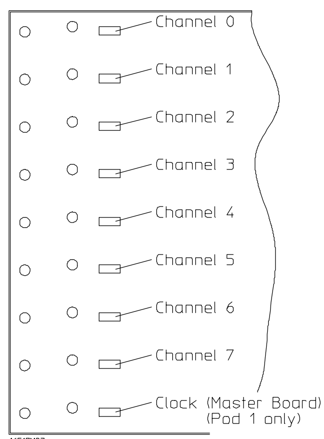
Verify the probe leads

1 Ground the oscilloscope probe lead to the barrel of the push-button ID switch. Set up the oscilloscope according to the following table:

Oscilloscope Setup

Channel 1	Horizontal	Trigger
V/Div 20 mV	s/Div 5.00 ns	–160 mV
Offset: –160 mV	Mode Realtime	

2 Probe the incoming signal at the circuit board bonding pads as shown. The signal should be approximately 100 mV in amplitude and –160 offset.



If a signal is not present then suspect a faulty probe lead. Replace the probe lead according to "To replace a probe lead" procedure in chapter 6.

If all signals are present, then proceed to Verify the pod.

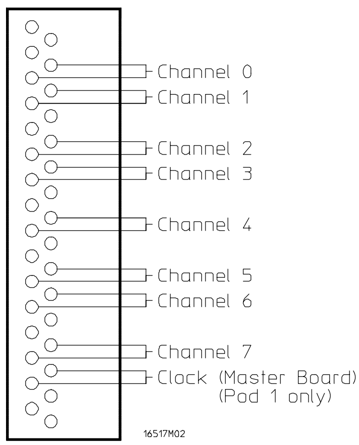
Verify the pod

1 Set up the oscilloscope according to the following table:

Oscilloscope Setup

Channel 1	Horizontal	Trigger
V/Div 100 mV	s/Div 5.00 nS	–400 mV
Offset -400 mV	mode realtime	

2 Probe all of the probe channels at the pod cable connector as indicated in the figure below. The signal will be approximately 600 mV in amplitude and -400 mV offset.



If a signal is not found then suspect a faulty pod assembly. Replace the pod assembly according to "To replace a pod" procedures in chapter 6.

If all signals are present, then proceed to Verify the cable.

Verify the cable

1 Remove power from the mainframe and remove the board with the suspect pod from the mainframe. Disconnect both pod cables from the board, swap the cables, and reinstall the cables onto the board.

2 Reinstall the board in the mainframe and apply power. If the problem follows the pod, then replace the probe cable of the suspect pod. If the problem remains where it was originally found, then swap the circuit board.

3 Remove power from the mainframe. Reassemble the pod clamshell. Ensure that the probe cable and the probe lead strain reliefs are properly inserted in the clamshell slots.

6

Replacing Assemblies

Replacing Assemblies

This chapter contains the instructions for removing and replacing the logic analyzer module, the circuit board of the module, and the probe cables of the module. Also in this chapter are instructions for returning assemblies.

CAUTION Turn off the instrument before installing, removing, or replacing a module in the instrument. Failure to do so could damage the equipment.

Tools Required

A T10 TORX screwdriver is required to remove screws connecting the probe cables and screws connecting the back panel.

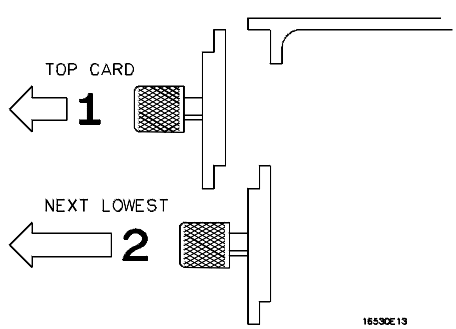
To remove the module

CAUTION Electrostatic discharge can damage electronic components. Use grounded wriststraps and mats when performing any service to this module.

1 Turn off the instrument power switch, then unplug the power cord. Disconnect any input or output connections.

2 Loosen the thumb screws.

Starting from the top, loosen the thumb screws on the filler panels and cards located above the module and the thumb screws of the module.



3 Starting from the top, pull the cards and filler panels located above the module halfway out.

4 If the module consists of a single card, pull the card completely out. Then go to the next page, "To replace the module."

If the module consists of more than one card, pull the complete module approximately halfway out.

5 Push all other cards into the card cage, but not completely in.

This is to get them out of the way for removing and replacing the module or a card in the module.

6 Starting with the top card in the module, disconnect the intercard cable, then slide the card completely out. Remove each card in the same manner until the faulty card is removed. Then go to the next page, "To replace the module."

To replace the module

1 If the module consists of a single card, slide the card approximately halfway into the mainframe, then go to step 2.

If the module consists of more than one card, perform the following steps:

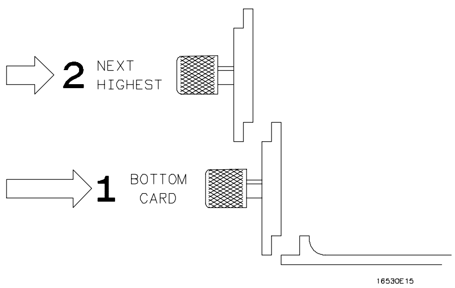
a Slide the card approximately halfway into the mainframe.

b Feed the intercard cable up through the slot in the card, then connect the cable to the card.

Repeat steps a and b for the remaining cards of the module.

c Slide the cards above the slots for the module about halfway out of the mainframe.

2 Starting with the bottom card, position all cards and filler panels so that the endplates overlap.



3 Seat the cards and tighten the thumbscrews.

Starting with the bottom card, firmly seat the cards into the backplane connector of the mainframe. Keep applying pressure to the center of the card endplate while tightening the thumbscrews finger-tight. Repeat this for all cards and filler panels starting at the bottom and moving to the top.

CAUTION For correct air circulation, filler panels must be installed in all unused card slots. Correct air circulation keeps the instrument from overheating. Keep any extra filler panels for future use.

To replace the circuit board

1 Remove the faulty card, then lay the card on an antistatic mat. Refer to "To remove the module" for the removal procedure.
2 Remove the two screws connecting each probe cable retainer to the circuit board, then remove the retainer.
3 Remove the four screws connecting the endplate to the circuit board, then remove the endplate and the ground spring.
4 Remove the probe cable from the connector on the circuit board, then connect the probe cable to the connector on the replacement circuit board.
5 Position the ground spring and back panel on the back edge of the replacement circuit board. Install the four screws to connect the back panel and ground spring to the circuit board.
6 Position the probe cable retainer on the circuit board, then install the two screws connecting each retainer to the circuit board.
7 Install the repaired module into the mainframe. Refer to "To replace the module" for the replacement procedure.

To replace a pod

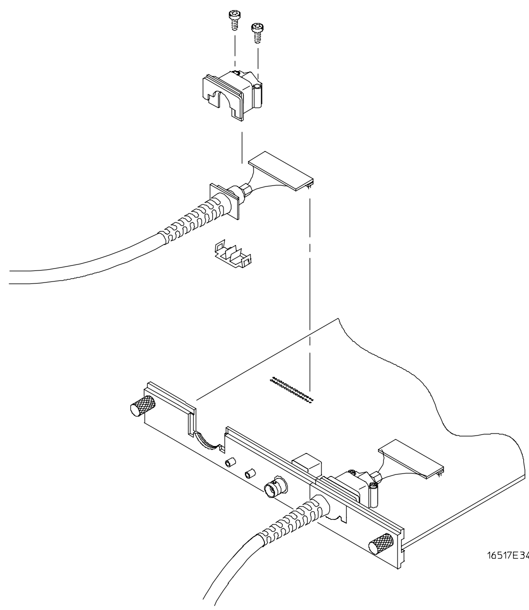
CAUTION The effects of ELECTROSTATIC DISCHARGE can damage electronic equipment. Use grounded wrist straps and mats when you are performing any kind of service to the pods and pod cables.

1 Using a Torx 10 screwdriver, remove 4 screws holding the clamshell pod case together of both the new pod and the faulty pod.
2 Lift the top off of the clamshell pod case of both the new pod and the faulty pod.
3 Gently unplug the cable from the pod assembly circuit board of the faulty pod. Use a small screwdriver to slowly lift the cable plug from the socket in the pod circuit board. Use caution to not bend any of the pins on the pod cable plug.
4 Plug the pod cable into the new pod assembly. Gently press down on the top of the pod cable plug to ensure the plug is firmly seated in the socket on the pod circuit board.
5 Reassemble the pod. Ensure that the pod cables and the probe leads are seated in the proper slots in the clamshell pod case.

To replace a pod cable

CAUTION The effects of ELECTROSTATIC DISCHARGE can damage electronic equipment. Use grounded wrist straps and mats when you are performing any kind of service to the pods and pod cables.

1. Follow the procedure "To remove the module". If the faulty pod cable resides on an expander board, separate the expander board from the rest of the module.
2. Using a Torx 10 screwdriver, remove 4 screws holding the clamshell pod case together.
3. Lift the top off of the clamshell pod case of the pod assembly.
4. Using a Torx 10 screwdriver, remove the rear panel cable clamp from the acquisition board assembly.

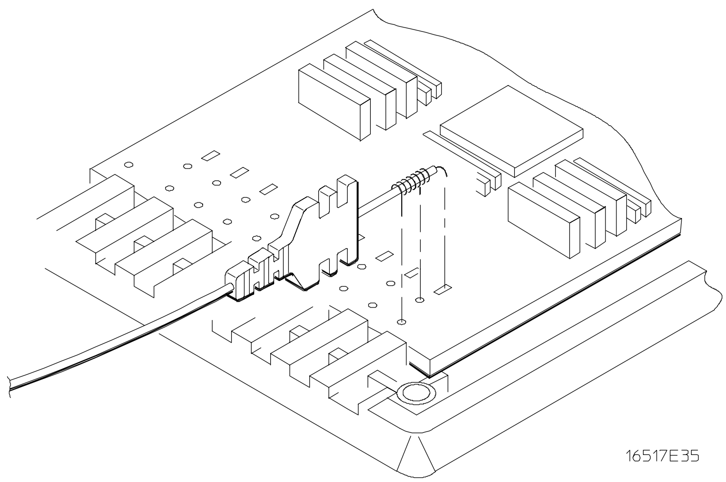


5. Gently unplug the faulty cable from the pod assembly circuit board. Use a small screwdriver to slowly lift the cable plug from the socket in the pod circuit board. Use caution to not bend any of the pins on the pod cable plug.
6. Gently unplug the faulty cable from the acquisition circuit board. Use a small screwdriver to slowly lift the cable plug from the socket in the acquisition circuit board. Use caution to not bend any of the pins on the pod cable plug.
7. Plug the new pod cable into the pod assembly. Gently press down on the top of the pod cable plug to ensure the plug is firmly seated in the socket on the pod circuit board.
8. Plug the new pod cable into the acquisition board. Gently press down on the top of the pod cable plug to ensure the plug is firmly seated in the socket on the acquisition circuit board.
9. Reassemble the pod. Ensure that the pod cables and the probe leads are seated in the proper slots in the clamshell pod case.
10. Reinstall the rear panel cable clamp on the acquisition board assembly. If the faulty pod resided on an expander board, reinstall the expander board into the module. Reinstall the module into the frame.

To replace a probe lead

Replacing a probe lead requires skill with a soldering iron. A low-wattage soldering iron is preferred to perform this task. Contact your nearest Agilent Technologies service center if you do not have the skill or resources to perform this task.

1 Using a Torx 10 screwdriver, remove 4 screws holding the clamshell pod case together.
2 Liftoff the top of the clamshell pod case of the pod assembly.



3 Using a soldering iron, unsolder the center conductor wire of the faulty probe lead from the bonding pad on the pod circuit board.
4 With a pair of needle nosed pliars, unplug the ground connector spring from the pod circuit board and lift the faulty probe lead away from the pod assembly.
5 Flow enough solder onto the vacant solder pad for a good solder joint.
6 Remove the color code clip from the faulty probe lead and insert the clip onto the new probe lead.
7 Insert the probe ground spring legs into the circuit board pin sockets.
8 While holding the probe ground spring in place, place the notched strain relief in the slot of the lower half of the clamshell cover.
9 Re-flow the solder on the vacant solder joint and install the probe lead center conductor in the flowed solder. The resulting solder joint should be very similar to the other probe leads.
10 Inspect the solder joint for good soldering integrity.

To return assemblies

Before shipping the module to Agilent Technologies, contact your nearest Agilent Technologies sales office for additional details.

1 Write the following information on a tag and attach it to the module.

- Name and address of owner
- Model number
- Serial number
- Description of service required or failure indications

2 Remove accessories from the module.

Only return accessories to Agilent Technologies if they are associated with the failure symptoms.

3 Package the module.

You can use either the original shipping containers, or order materials from an Agilent Technologies sales office.

CAUTION Electrostatic discharge can damage electronic components. For protection against electrostatic discharge, package the module in electrostatic material.

4 Seal the shipping container securely, and mark it FRAGILE.

Replaceable Parts

Replaceable Parts

This chapter contains information for identifying and ordering replaceable parts for your logic analyzer.

Replaceable Parts Ordering

Parts listed

To order a part on the list of replaceable parts, quote the Agilent Technologies part number, indicate the quantity desired, and address the order to the nearest Agilent Technologies Sales Office.

Parts not listed

To order a part not on the list of replaceable parts, include the model number and serial number of the module, a description of the part (including its function), and the number of parts required. Address the order to your nearest Agilent Technologies Sales Office.

Direct mail order system

To order using the direct mail order system, contact your nearest Agilent Technologies Sales Office.

Within the USA, Agilent Technologies can supply parts through a direct mail order system. The advantages to the system are direct ordering and shipment from the Agilent Technologies Part Center in Mountain View, California. There is no maximum or minimum on any mail order. (There is a minimum amount for parts ordered through a local Agilent Technologies Sales Office when the orders require billing and invoicing.) Transportation costs are prepaid (there is a small handling charge for each order) and no invoices.

In order for Agilent Technologies to provide these advantages, a check or money order must accompany each order. Mail order forms and specific ordering information are available through your local Agilent Technologies Sales Office. Addresses and telephone numbers are located in a separate document at the back of the service guide.

Exchange Assemblies

Some assemblies are part of an exchange program with Agilent Technologies.

The exchange program allows you to exchange a faulty assembly with one that has been repaired and performance verified by Agilent Technologies.

After you receive the exchange assembly, return the defective assembly to Agilent Technologies. A United States customer has 30 days to return the defective assembly. If you do not return the defective assembly within the 30 days, Agilent Technologies will charge you an additional amount. This amount is the difference in price between a new assembly and that of the exchange assembly. For orders not originating in the United States, contact your nearest Agilent Technologies Sales Office for information.

See Also "To return assemblies," in chapter 6.

Replaceable Parts List

The replaceable parts list is organized by reference designation and shows exchange assemblies, electrical assemblies, then other parts.

The exploded view does not show all of the parts in the replaceable parts list.

Information included for each part on the list consists of the following:

- Reference designator
- Agilent Technologies part number
- Total quantity included with the instrument (Qty)
- Description of the part

Reference designators used in the parts list are as follows:

- A Assembly
- H Hardware
- MP Mechanical Part
- W Cable

Agilent Technologies 16517A Replaceable Parts

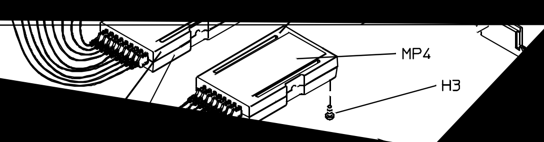
Ref. Des.	Agilent Part Number	QTY	Description
Exchange Assembly			
	16517-69509	1	Exchange Circuit Board
Replacement Parts			
	0510-0684	2	Retaining Ring
	0515-0430	4	MSPH M3.0x0.50 6mm T10
	0515-0666	4	MSPH M3.0x0.50 18mmT10
	0535-0006	1	Hex Nut M4x0.7
	0624-0729	2	Tapping Screw - 2-56
	16500-22401	2	Panel Screw
	16517-09101	2	Spring Clamp
	16517-40501	1	Back Panel - Master Board
	16517-40502	2	Back Panel Clamp
	16517-66509	1	Circuit Board Assembly - Master
	16517-94301	1	ID Label - Master Board
	16518-61601	2	Cable - Single Expander
	16518-61602	2	Cable - Double Expander
	16550-29101	1	Ground Spring
	8120-1840	1	Cable Assembly
Pod/Cable Assembly			
	0515-0658	2	MSPH M2.0x0.40 6mm T6 (Pod/Cable Assembly)
	0515-0664	4	MSPH M3.0x0.50 12mm T10 (Pod/Cable Assembly)
	16517-41203	1	Cable Marker - Black
	16517-41204	1	Cable Marker - Brown
	16517-41205	1	Cable Marker - Red
	16517-41206	1	Cable Marker - Orange
	16517-41207	1	Cable Marker - Yellow
	16517-41208	1	Cable Marker - Green
	16517-41209	1	Cable Marker - Blue
	16517-41210	1	Cable Marker - Violet
	16517-41211	1	Cable Marker - White
	16517-44101	1	Master Board Pod Clamshell - Top
	16517-44102	1	Master Board Pod Clamshell - Bottom
	16517-61601	1	Pod Cable - Master
	16517-63203	1	Master Probe Pod (with clock)
	16517-63205	1	Master Probe Pod (without clock)
	16517-94303	1	Master Board Pod 1 Label
	16517-94305	1	Master Board Pod 2 Label
	5081-7753	0	Replacement Probe Leads (Bag of 3 leads)
Master Board Accessory Kit			
	16517-68701	1	Master Board Accessory Kit
	16515-27601	2	Ground Connector
	16517-61604	1	CM - BNC Adapter Cable
	16517-63201	1	Calibration Pod
	16517-64501	1	Probe Kit Case
	16517-82104	1	SMT Leads (Qty 20)
	16517-82105	1	Ground Extender (Qty 20)
	16517-82106	1	Ground Lead (Qty 20)
	16517-82107	1	Pin Probe (Qty 4)
	16517-82108	1	Grabber (Qty 20)
	16517-94304	1	Accessory Kit Label

Agilent Technologies 16518A Replaceable Parts

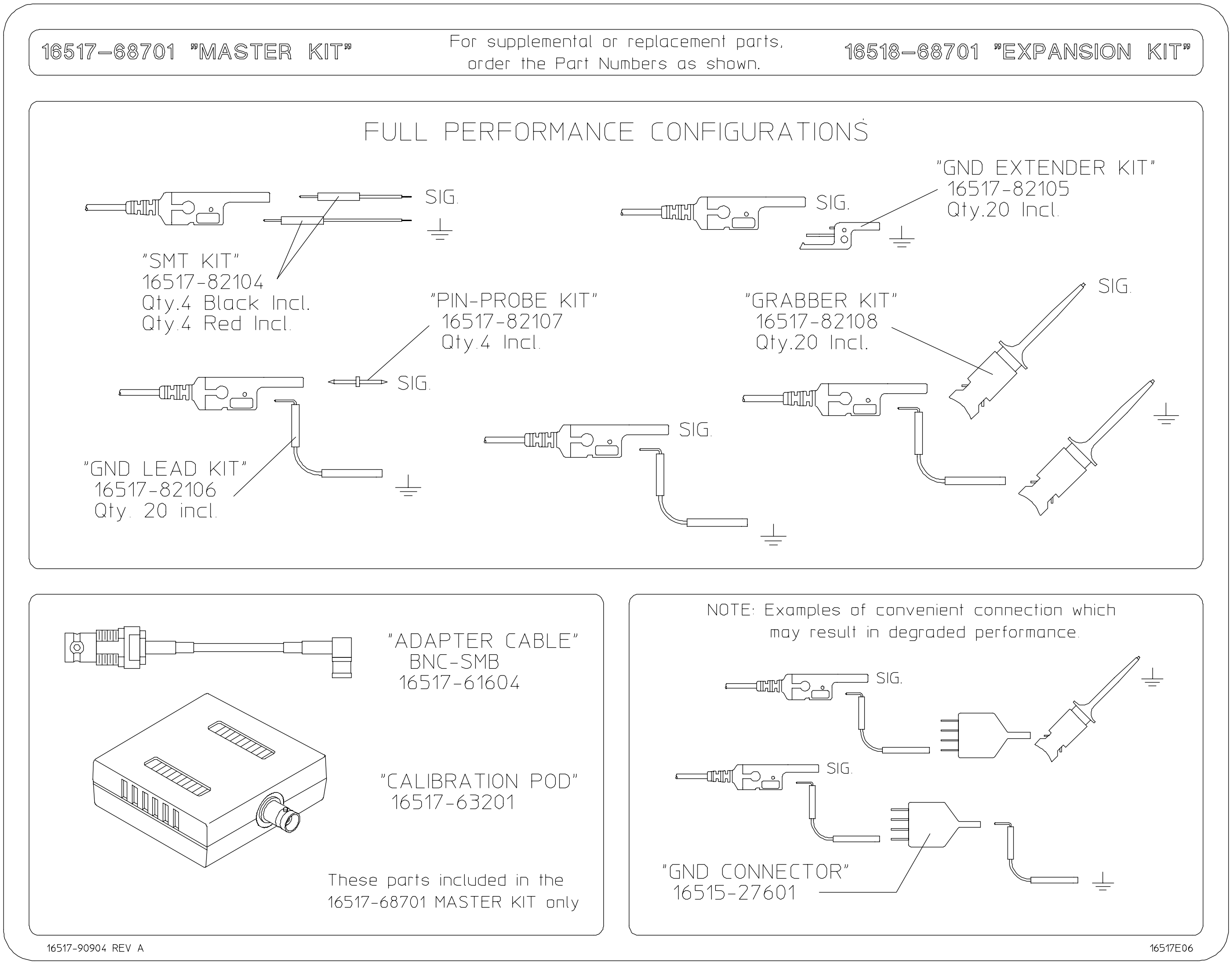
Ref. Des.	Agilent Part Number	QTY	Description
Exchange Assembly			
	16518-69501	1	Exchange Circuit Board
Replacement Parts			
	0510-0684	2	Retaining Ring

Agilent Technologies 16518A Replaceable Parts

Ref. Des.	Agilent Part Number	QTY	Description
	0515-0430	4	MSPH M3.0x0.50 6mm T10
	0515-0666	4	MSPH M3.0x0.50 18mmT10
	16500-22401	2	Panel Screw
	16517-09101	2	Spring Clamp
	16517-40502		Back Panel Clamp
	16518-40501	1	Back Panel - Expander Board
	16518-66501	1	Circuit Board Assembly - Expander
	16518-94301	1	ID Label - Expander Board
	16550-29101	1	Ground Spring
Pod/Cable Assembly			
	0515-0658	2	MSPH M2.0x0.40 6mm T6 (Pod/Cable Assembly)
	0515-0664	4	MSPH M3.0x0.50 12mm T10 (Pod/Cable Assembly)
	16517-41203	1	Cable Marker - Black
	16517-41204	1	Cable Marker - Brown
	16517-41205	1	Cable Marker - Red
	16517-41206	1	Cable Marker - Orange
	16517-41207	1	Cable Marker - Yellow
	16517-41208	1	Cable Marker - Green
	16517-41209	1	Cable Marker - Blue
	16517-41210	1	Cable Marker - Violet
	16517-44101	1	Expander Board Pod Clamshell - Top
	16517-44102	1	Expander Board Pod Clamshell - Bottom
	16518-44101	1	Expander Pod Clock Plug
	16518-61603	2	Pod Cable - Expander
	16518-63202	0	Expander Probe Pod
	16518-94302	1	Expander Board Pod Label
	5081-7753	0	Replacement Probe Leads (Bag of 3 leads)
Expander Board Accessory Kit			
	16518-68701	1	Expander Board Accessory Kit
	16515-27601	2	Ground Connector
	16517-64501	1	Probe Kit Case
	16517-82104	1	SMT Leads (Qty 20)
	16517-82105	1	Ground Extender (Qty 20)
	16517-82106	1	Ground Lead (Qty 20)
	16517-82107	1	Pin Probe (Qty 4)
	16517-82108	1	Grabber (Qty 20)
	16517-94304	1	Accessory Kit Label


MP4
H3

Accessory Kit



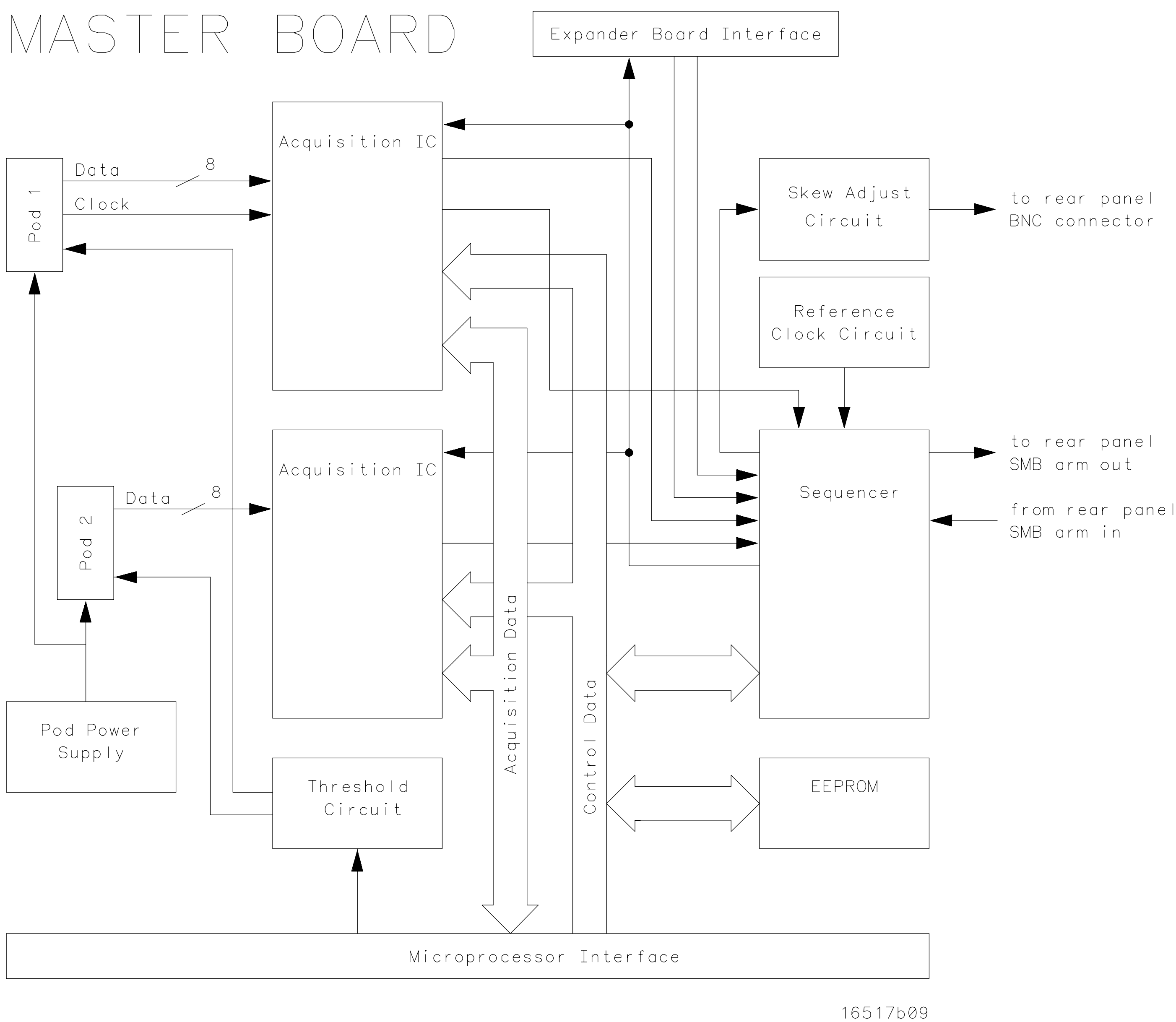
Accessory Kit

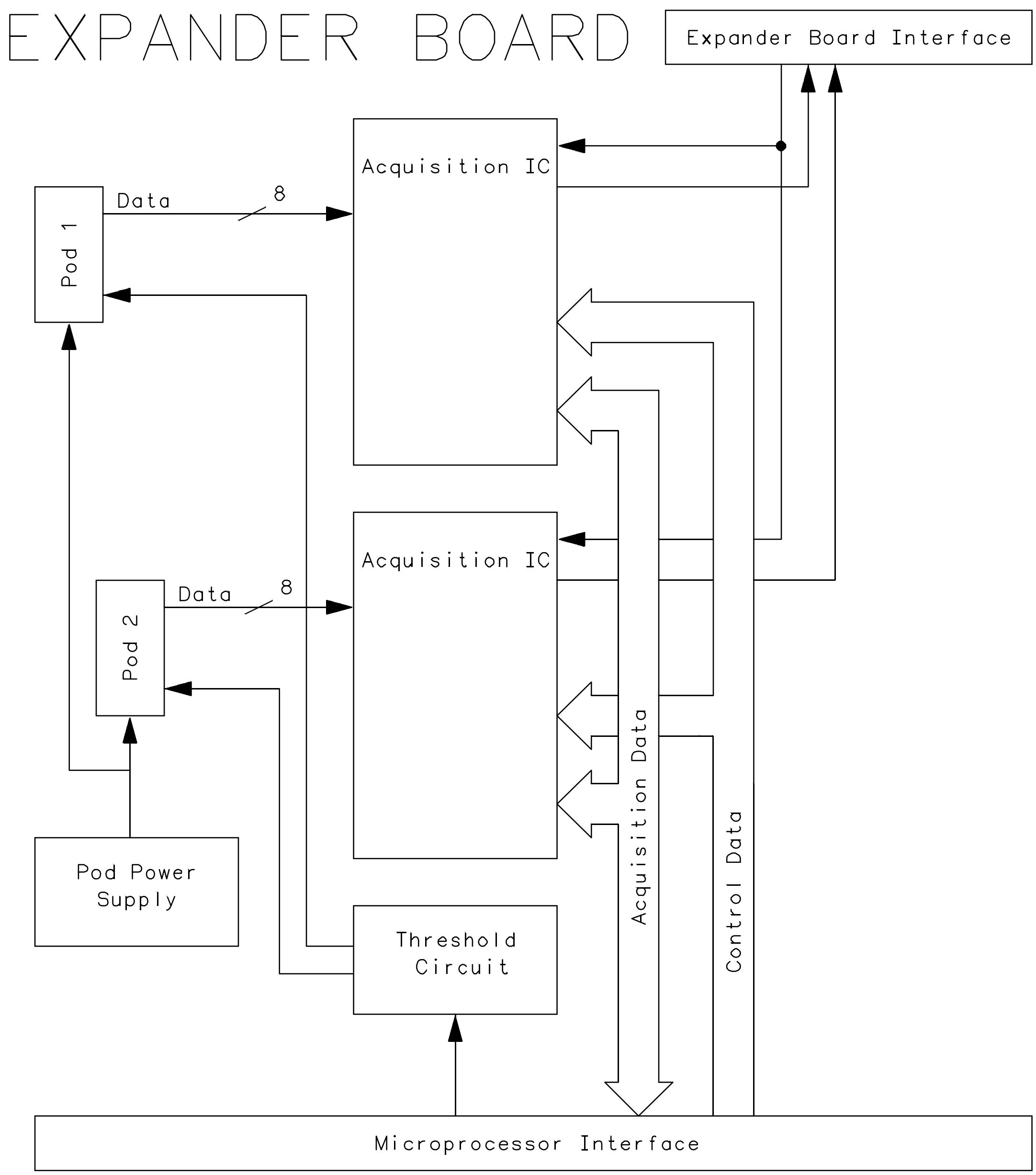
Theory of Operation

Theory of Operation

This chapter tells the theory of operation for the logic analyzer and describes the operation verification tests. The information in this chapter is to help you understand how the logic analyzer operates and what the operation verification tests are testing. This information is not intended for component-level repair.

The following two illustrations show the block-level diagrams of the master card and the expander card. Refer to these illustrations for the descriptions under Block Level Theory.




EXPANDER BOARD
Expander Board Interface
Acquisition IC
Data
8
Pod 1
Acquisition IC
Data
8
Pod 2
Pod Power Supply
Threshold Circuit
Acquisition Data
Control Data
Microprocessor Interface

16517b10

Both the master board and expander board of the 16517A/18A Data Acquisition module operate identically with a few exceptions, which are explained below.

Pod 1, Pod 2 (Master Board and Expander Board)

Two 8-channel data acquisition pods are available on both the 16517A master board and 16518A expander board. For synchronous acquisition of data (state analysis), Pod 1 of the master board has one clock channel. For proper operation of synchronous data acquisition, the clock pulse being fed to the master board pod 1 clock channel must be periodic.

The data acquisition pods are each made up of a comparator IC in a clamshell housing at the end of the pod cable. The comparator sends the target system signal data to the data acquisition module as double-ended signals for greater noise immunity. Power for the pod comparator is supplied by the data acquisition module through the pod cable.

A momentary push button on the side of the pod sends an identification signal which is read by the microprocessor interface. The signal is routed from the microprocessor interface to the Agilent Technologies 16500A,B mainframe, and the mainframe then interprets the signal and displays the origin of the identification signal as a green bar message on the monitor.

Threshold Circuit (Master Board and Expander Board)

A proprietary 15-channel DAC supplies threshold voltage information to the comparator ICs in the pods through the pod cables. The threshold for each pod can be set independent of the threshold voltages of the other pods. Both the master board and the expander board have their own DACs which operate independently when the master and expander boards are configured together.

Acquisition ICs (Master Board and Expander Board)

Two acquisition ICs on both the master board and expander board are multi-chip modules (MCM) containing all of the circuitry necessary to acquire and store data. An encoder, FISO, and pattern RAM are on the acquisition IC. Additionally, a phase locked loop on the acquisition IC controls the sample rate of the acquisition.

The encoder channels the acquired data to the proper locations in the FISO. The pattern RAM stores the user-programmed pattern resource information. The output signal lines of the pattern RAM are directed to the Sequencer IC. When an acquired pattern matches one of the programmed pattern resources for a particular label, then the appropriate pattern RAM output line is asserted and the sequencer moves to the next programmed sequence level.

Sequencer (Master Board only)

The sequencer, the state machine that controls the data acquisition, is made up of a proprietary programmable device. All of the pattern resource information, module arming, and IMB arming and triggering is handled by the sequencer.

The sequencer also channels an ECL level arming signal to the rear panel SMB arm out connector of the master board. The rear panel SMB arm in connector directs an ECL-level arming signal to the sequencer. The arm in connector is terminated into 50 ohms.

Reference Clock Circuit (Master Board only)

The reference clock circuit provides a 62.5 MHz reference signal to the acquisition ICs. For timing analysis, the acquisition ICs feed this reference signal to a phase locked loop. The phase locked loop steps this signal to the desired data sampling frequency, up to 4 GHz.

The reference signal is also directed to the operational accuracy calibration circuit. In this case, the reference signal is used to optimize the performance of the 16517A/18A module.

Skew Adjust Circuit (Master Board only)

The skew adjust circuit is made up of a single line driver which drives the calibration output BNC on the rear panel of the master board. The line driver provides a very fast rise time signal which is used to optimize the channel-to-channel skew.

EEPROM (Master Board only)

The EEPROM stores the calibration factors obtained during an operational accuracy calibration. A calibration protect switch on the master board prevents the calibration factors from being accidently over-written.

Expander Board Interface

The expander board interface is made up of line drivers and interboard cabling. Using line drivers on the expander boards, pattern resource information is directed to the master board from all of the connected expander boards. Run control information is likewise directed to the expander boards from the master board. Consequently, the acquisition ICs on the expander board are controlled in parallel from the master board.

Description of Operation Verification Tests

The Operation Verification Tests are divided into two main menus: Functional Tests and Skew Dependent Tests. The Functional Tests do not require connection of each pod to the calibration port on the rear panel of the master board. Using internal clocking and data routing, the main components in the clock and data pipelines are functionally tested to ensure they operate. This ensures that clock and data signals can propagate through the 16517A/18A circuitry.

The Skew Dependent Tests require current skew factors either by loading the skew factors from memory or performing a skew adjust. If the 16517A/18A module is being performance verified at the two-year performance verification interval, then performing a skew adjust is recommended.

If expander boards are configured with the master board, the circuitry on each of the expander boards is tested at the same time as the circuitry on the master board. There are no tests that are specific to either the master board or expander board.

Functional Tests

The Functional Tests verify correct operation of the main subsystems of the 16517A/18A module. Though no parametric tests are performed during the functional tests, the performance of the 16517A/18A module is examined.

Data Memory Test

The data memory test exercises the memory fast-in-slow out (FISO) memory on board the acquisition IC. This test is integrated into the data memory FISO itself. When executed, a checkerboard pattern of 1's and 0's is loaded into the FISO and then read.

Passing the data memory test implies that the acquisition memory is operating properly and is able to store either a logic 1 or a logic 0 at each memory location. Failure of this test indicates a problem with the FISO memory on the acquisition IC.

Probe Data Acq Test

The Probe Data Acquisition Test verifies the correct operation of the acquisition data pipeline of the 16517A/18A module. The comparator threshold is first configured for either of the -5.00 vDC and +5.00 vDC limits. Because the voltage at the probe tip is floating at ground, a logic 1 or a logic 0 is artificially asserted.

Signal routing circuitry in the acquisition IC permits directing the probe data to some of the pod channels while directing internal test data through the remaining pod channels. Consequently, some channels are passing the artificially asserted logic level while the other channels are passing test data. After setting the pod threshold to the lower threshold limit, test data is directed to four pod channels while the asserted logic 1 is read on the other four channels. The resulting data is then read and compared with expected values. The pod threshold is then set to the upper threshold limit, and the resulting logic 0 that is asserted on the eighth channel is combined in parallel with the test data appearing on the other seven channels. The resulting data is again read and compared with expected values. Each of the eight pod channels pass artificially asserted logic levels after which the resulting data is read and compared with expected values. Several channels and probe level combinations are run to verify channel functionality and independence.

Passing the Probe Data Acq Test implies that all pod channels in the acquisition data pipeline can properly transport either a logic 1 or a logic 0 to the acquisition memory. Passing this test also implies that each channel is electrically isolated from adjacent channels. Failure of this test indicates a problem with the comparator in the probe pod, the cable, or the 16517A/18A module circuit board.

Half Ch Mode Test

The Half Channel Mode Test verifies the correct operation of the multiplexers in the acquisition IC used during the 16517A/18A half channel mode of operation. Pod data is artificially created by setting the pod threshold to the threshold limits for four channels. The pod data is then combined with test data fed to the remaining four channels in the same manner as in the Probe Data Acq Test. The multiplexers are then exercised, which routes the logic 1 or logic 0 from the pod in parallel with the test data to appropriate locations in the acquisition IC memory. The data routing is the same as the data routing done in the half-channel mode of operation.

The resulting patterns are then read and compared with expected values.

Passing the Half Ch Mode Test implies that the half channel mode multiplexers are operating properly. Passing this test also implies that each channel is electrically isolated from adjacent channels in the half channel mode of operation. Failure of this test indicates a problem with the multiplexers in the acquisition IC. Failure of this test and also the Probe Data Acq Test indicates that the data channels are not electrically isolated from each other. This failure is caused by a problem with either the comparator on the probe pod, the cable, or the 16517A/18A module circuit board.

High Speed Acq Test

The High Speed Acquisition Test verifies the correct operation of the high-speed acquisition clock pipeline (2 GSa/s, 1 GSa/s, and 500MSa/s acquisition clock speeds). The 16517A/18A module is configured for low-speed acquisition mode, which activates the low-speed acquisition clock pipeline. Test data is then routed through the high-speed acquisition clock pipeline and through the high-speed clock divider circuitry. The outputs of each of the high-speed clock dividing circuits is then read and compared with known values.

Passing the High Speed Acq Test implies that the high-speed acquisition clock pipeline and the corresponding clock divide-by-two circuitry are operating properly and will clock the 16517A/18A at high data acquisition rates. Failing the test implies that the 16517A/18A module will not be able to properly acquire data at high data rates because of a problem with the high-speed clock circuit.

Low Speed Acq Test

The Low Speed Acquisition Test verifies the correct divide-down operation of the low-speed acquisition clock pipeline. The 16517A/18A module is configured for high-speed acquisition mode, which activates the high-speed acquisition clock pipeline. Test data is then routed through the low-speed acquisition clock pipeline and through the clock divide-by-two circuitry. The outputs of each of the divide-by-two circuits is then read and compared with known values.

Passing the Low Speed Acq Test implies that the low-speed acquisition clock pipeline and the corresponding clock low-speed clock divider circuitry are operating properly, and will clock the 16517A/18A at low data acquisition rates. Failing the test implies that the

16517A/18A module will not be able to properly acquire data at low data rates because of the low-speed clock circuit.

Memory Clock Test

The Memory Clock Test operates the same as the Low Speed Acq Test, except the clock divide-by-two circuitry in the sequencer IC is exercised. The high-speed acquisition clock pipeline is again activated, and test data is passed through the low-speed acquisition clock pipeline. The outputs of each of the divide-by-two circuits in the sequencer IC is then read and compared with known values.

The sequencer IC itself is also test during the Memory Clock Test. Each of the sequence levels are activated and all of the possible sequence level branches are exercised in the sequencer.

Passing the Memory Clock Test implies that the sequencer itself is operating properly, and that the sequencer can be properly controlled by the both the acquisition IC and the module master clock. Failure of this test indicates a problem with the sequencer IC.

Skew Dependent Test

The Skew Dependent Test requires current skew factors in order to properly run the test. Current skew factors must be used, so there are two paths to the Skew Dependent Test. The first path requires performing a skew adjust on the module. The second path involves loading the skew factors from NV-RAM . In either case, valid skew factors are obtained, and consequently the 16517A/18A is performance optimized before running the Skew Dependent Test.

The Skew Adjust routines are also available as part of the Operation Verification tests as a troubleshooting and verification tool. If the 16517A,518A module can obtain skew factors for all pods, then there is reasonable confidence that the module will operate as expected. If the module is not able to obtain skew factors for a particular pod, then a hardware problem is likely and the module requires servicing.

Resource Xfer Test

The Resource Transfer Test verifies the correct operation of the pattern resources. Test data is used to generate patterns. The acquisition chip detects them and sends them to the sequencer via 1 of 4 resource transfer lines. The sequencer is configured to receive the expected patterns. The test fails if patterns are not detected by the acquisition chip, or if the sequencer does not receive them. Each pod is tested for each of 4 resource lines. There are 4 transfer modes for each line.

Passing the Resource Xfer Test implies that all pattern resources are properly operating, and that a match between the pattern resource information and the acquired data sends the appropriate signal to the 16517A/18A sequencer. Failure of this test indicates a problem with either the pattern resources on the acquisition IC, cables between boards, or the pattern resource circuitry between the acquisition IC and the sequencer.

Skew Adjust and Performance Verification Messages

The following Error, Warning, and Advisory messages may be encountered when performing the skew adjust or performance verification testing. Error messages have a red background and indicate that the measurement, or part of the measurement, will not occur until the problem is fixed. Warning messages have a yellow background, and indicate that the measurement, or part of the measurement may be at risk if the operation is not understood.

Error Messages

Measurement Did Not Complete. The user was adjusting skew or running a PV test that did not complete as it should have.

Could not complete fine deskew. Message will appear if the calibration was unable to complete the fine cal binary search.

Could not complete coarse deskew. Message appears if the calibration was unable to find the high and low values needed by the fine cal binary search.

Could not start deskew. Message appears if the calibration was unable to make the 1st acquisition needed to start the coarse cal.

Deskew Failed!. Message appears if the calibration did not find valid numbers.

Unable to find the leading/trailing edge. Message appears if the clock deskew can not identify the leading (rising clock) or trailing edge (falling clock).

get_acckdly_bits( ) failed. Message appears if the 2nd clock offset can not be set to the desired value.

Warning Messages

Skew adjustment halted, recalling stored values. This message appears when calibration is halted before the calibration is completed.

Skew adjustment failed, recalling stored values. This message appears when any calibration fails.

Skew adjustment failed. Press \"Proceed\" to retry or \"Exit\" to quit. This message appears when any calibration fails, but only before the user retries or quits.

16517/18 Skew values do not match HW configuration. The hardware configuration corresponding to the cal factors stored do not match the current configuration in the frame.

Using Default 16517/18 Skew Values. Please See \"Skew Adjust\" Menu. Since no valid Cal values were found in Flash ROM, or those read do not match the current HW, the Default Cal values are being loaded. The board skews should be re-adjusted.

Advisory Messages

Previous configuration: A:16518 B:16518 C:16517 D:16518 E:16518. This message describes the configuration that produced the stored cal factors. String is built on the fly.

Please adjust the skew or re-configure the module. This message appears after CAL_HW_MISMATCH, CAL_CONFIG and DFT_CAL_MSG are putup.

The clock is not connected properly. This message appears if code is unable to measure a signal on the clock as part of cal process.

Data channels (........) are not connected properly. This message appears if code is unable to measure a signal on any of the data channels as part of cal process. The string is built on the fly.

Warning Messages

Calibration halted, recalling stored values. This message appears when deskew is halted before the deskew is completed.

Pod may be incorrectly connected to stimulus port. If this message appears, it is most likely that the user has incorrectly connected a pod or pods to a stimulus port. This message warns the user of this. It is possible that the pod is in fact bad. If this is the case, the user should, after verifying the cable connections, assume that the hardware is defective.

Calibration failed, recalling stored values. This message appears when any deskew fails.

Current setup lost if calibration continued. This message appears when deskew starts.

16517/18 Skew values do not match hardware. The hardware configuration corresponding to the cal factors stored do not match the current configuration in the frame. Default Cal values are loaded.

Using Default 16517/18 Skew Values. Since no valid Cal values were found in Flash ROM, or those read do not match the current hardware, the Default Cal values are being loaded.

Starting clock offset normalization. This message appears when the 1 shot calibration starts.

Starting the clock to data deskew. This message appears when the clock deskew calibration starts.

Starting the data to data deskew. This message appears when the ch-ch deskew starts.

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Safety

This apparatus has been designed and tested in accordance with IEC Publication 348, Safety Requirements for Measuring Apparatus, and has been supplied in a safe condition. This is a Safety Class I instrument (provided with terminal for protective earthing). Before applying power, verify that the correct safety precautions are taken (see the following warnings). In addition, note the external markings on the instrument that are described under "Safety Symbols."

Warning

- Before turning on the instrument, you must connect the protective earth terminal of the instrument to the protective conductor of the (mains) power cord. The mains plug shall only be inserted in a socket outlet provided with a protective earth contact. You must not negate the protective action by using an extension cord (power cable) without a protective conductor (grounding). Grounding one conductor of a two-conductor outlet is not sufficient protection.
- Only fuses with the required rated current, voltage, and specified type (normal blow, time delay, etc.) should be used. Do not use repaired fuses or short-circuited fuseholders. To do so could cause a shock of fire hazard.
- Service instructions are for trained service personnel. To avoid dangerous electric shock, do not perform any service unless qualified to do so. Do not attempt internal service or adjustment unless another person, capable of rendering first aid and resuscitation, is present.
- If you energize this instrument by an auto transformer (for voltage reduction), make sure the common terminal is connected to the earth terminal of the power source.
- Whenever it is likely that the ground protection is impaired, you must make the instrument inoperative and secure it against any unintended operation.
- Do not operate the instrument in the presence of flammable gasses or fumes. Operation of any electrical instrument in such an environment constitutes a definite safety hazard.
- Do not install substitute parts or perform any unauthorized modification to the instrument.
- Capacitors inside the instrument may retain a charge even if the instrument is disconnected from its source of supply.
- Use caution when exposing or handling the CRT. Handling or replacing the CRT shall be done only by qualified maintenance personnel.

Safety Symbols

Instruction manual symbol: the product is marked with this symbol when it is necessary for you to refer to the instruction manual in order to protect against damage to the product.

Hazardous voltage symbol.

Earth terminal symbol: Used to indicate a circuit common connected to grounded chassis.

WARNING

The Warning sign denotes a hazard. It calls attention to a procedure, practice, or the like, which, if not correctly performed or adhered to, could result in personal injury. Do not proceed beyond a Warning sign until the indicated conditions are fully understood and met.

CAUTION

The Caution sign denotes a hazard. It calls attention to an operating procedure, practice, or the like, which, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the product. Do not proceed beyond a Caution symbol until the indicated conditions are fully understood or met.

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About this edition

This is the *Agilent Technologies 16517A/18A 4 GSa/s Timing and 1 GSa/s Synchronous State Logic Analyzer Service Guide*.

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New editions are complete revisions of the manual. Update packages, which are issued between editions, contain additional and replacement pages to be merged into the manual by you. The dates on the title page change only when a new edition is published.

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The following list of pages gives the date of the current edition and of any changed pages to that edition.

All pages original edition